

Compal Confidential

KALG1 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2009-03-02

REV 02

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/11/10	Deciphered Date	2008/11/24	Title	Cover Page
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File Name : LA-5271P

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Compal Electronics, Inc.

Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75VS power rail for DDR3 terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for NB(LVDS)	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3V	3.3V power rail for SB	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail for SB	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 100X b

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS367, SLG8SP556V)	1101 001Xb
DDR3 DIMMA	1001 000Xb
DDR3 DIMMB	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1				
2				
3				
4				
5				
6				
7				

BOARD ID Table




Board ID	PCB Revision
0	PCB 08Y LA-5271P REV0 M/B
1	
2	
3	
4	
5	
6	
7	

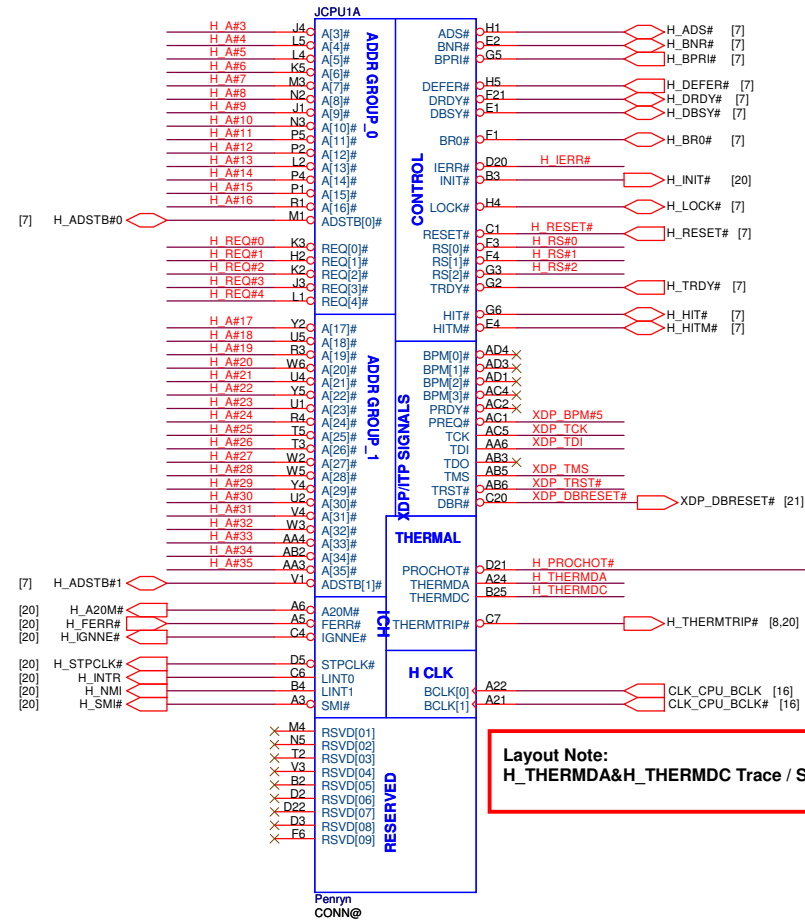
BTO Option Table

BTO Item	BOM Structure
GL40	GL40@
GM45	GM45@

BOM Configuration Table

Project	BOM Configuration
KALG1-GM45	GM45@/KALG1@/KAL90_G0_90+@
KALG1-GL40	GL40@/KALG1@/KAL90_G0_90+@

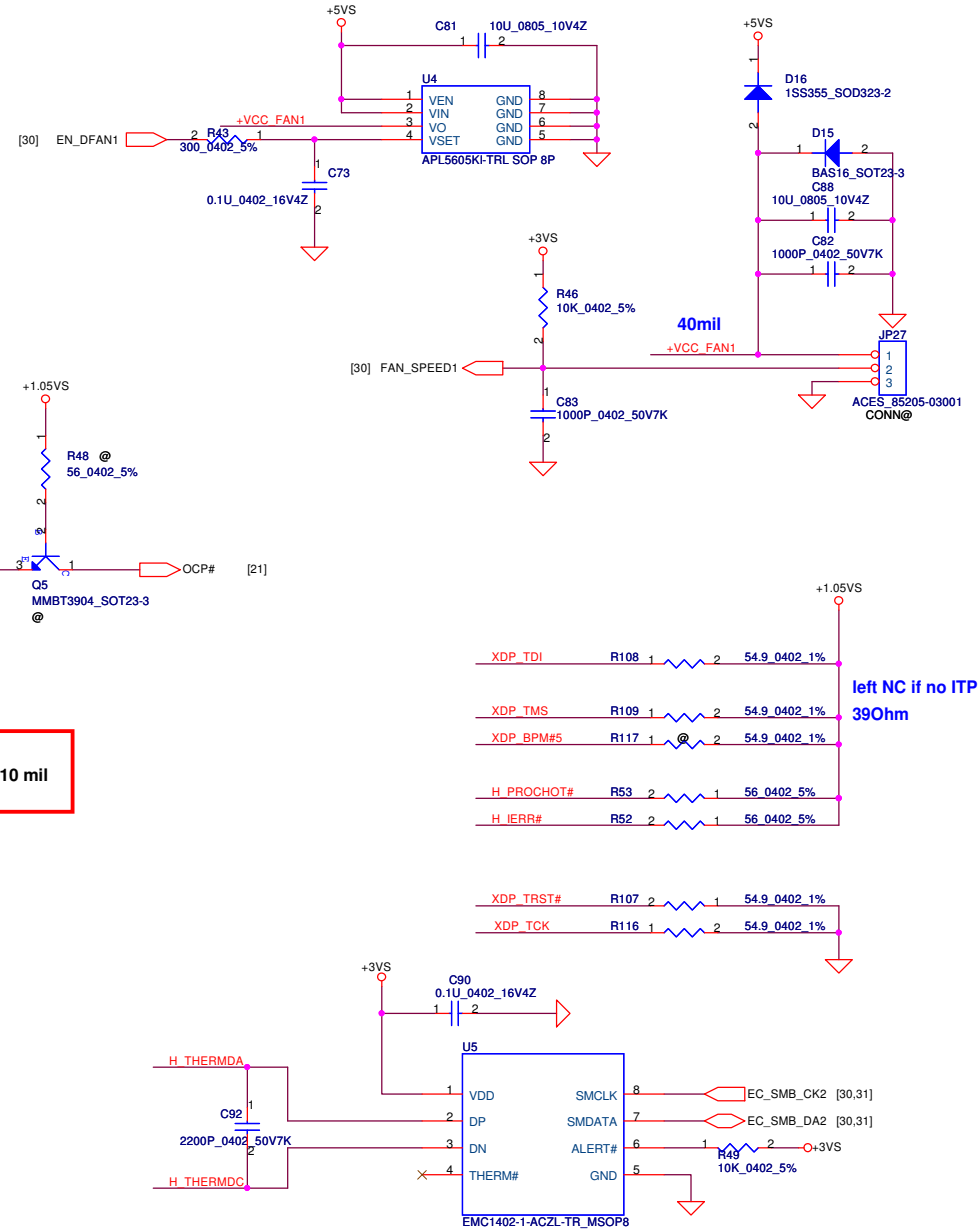
[7] H_A# [3..35]  H_A# [3..35]
 [7] H_REQ# [0..4]  H_REQ# [0..4]
 [7] H_RS# [0..2]  H_RS# [0..2]



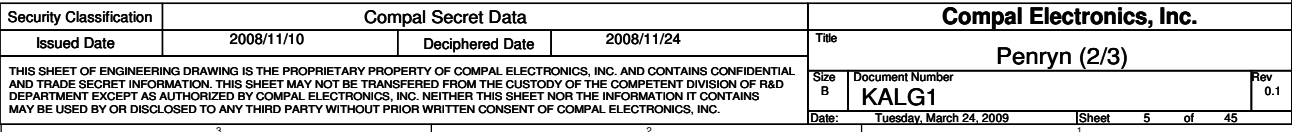
Layout Note:
 H_THERMDA&H_THERMDC Trace / Space = 10 / 10 mil

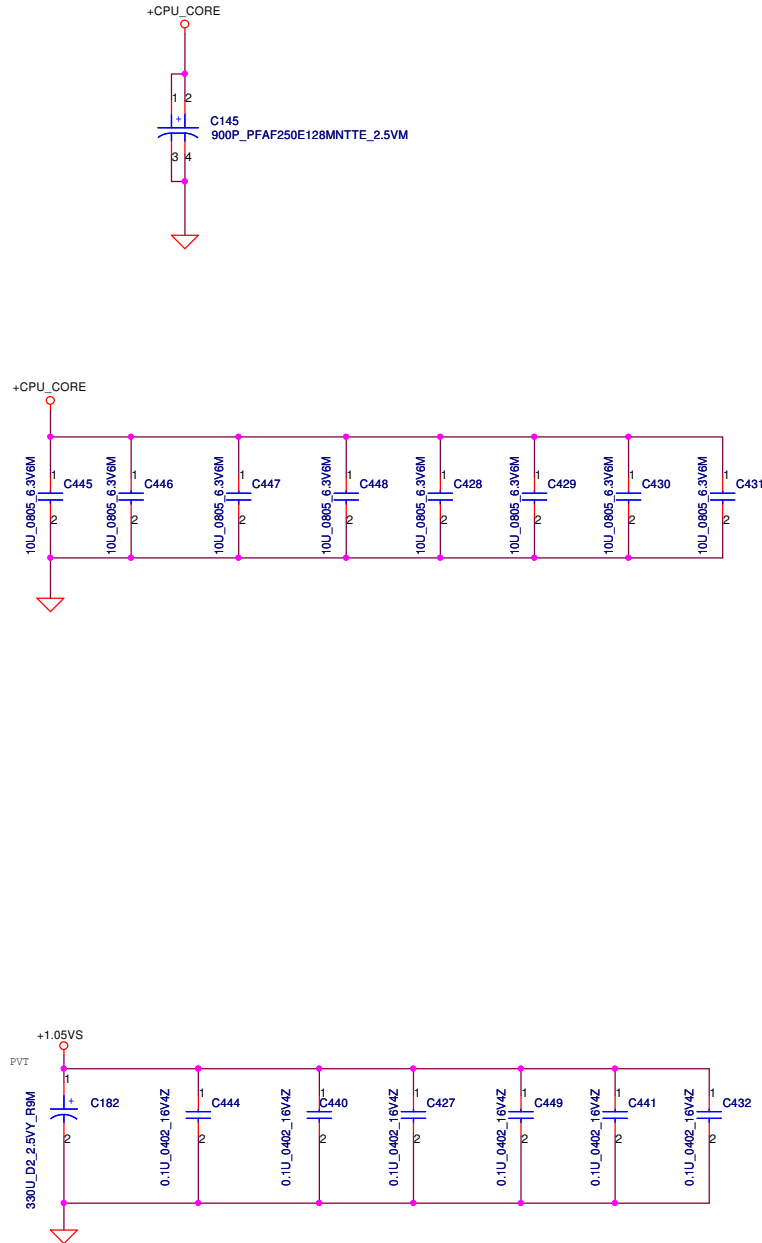
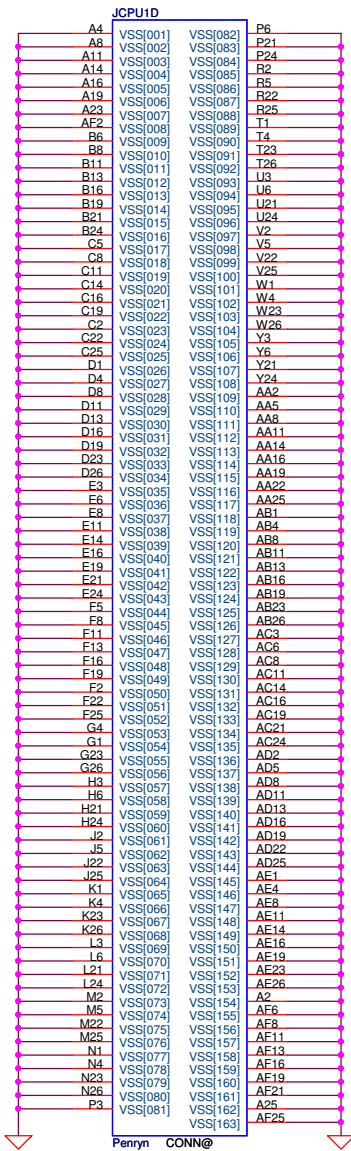
BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

FAN1 Conn

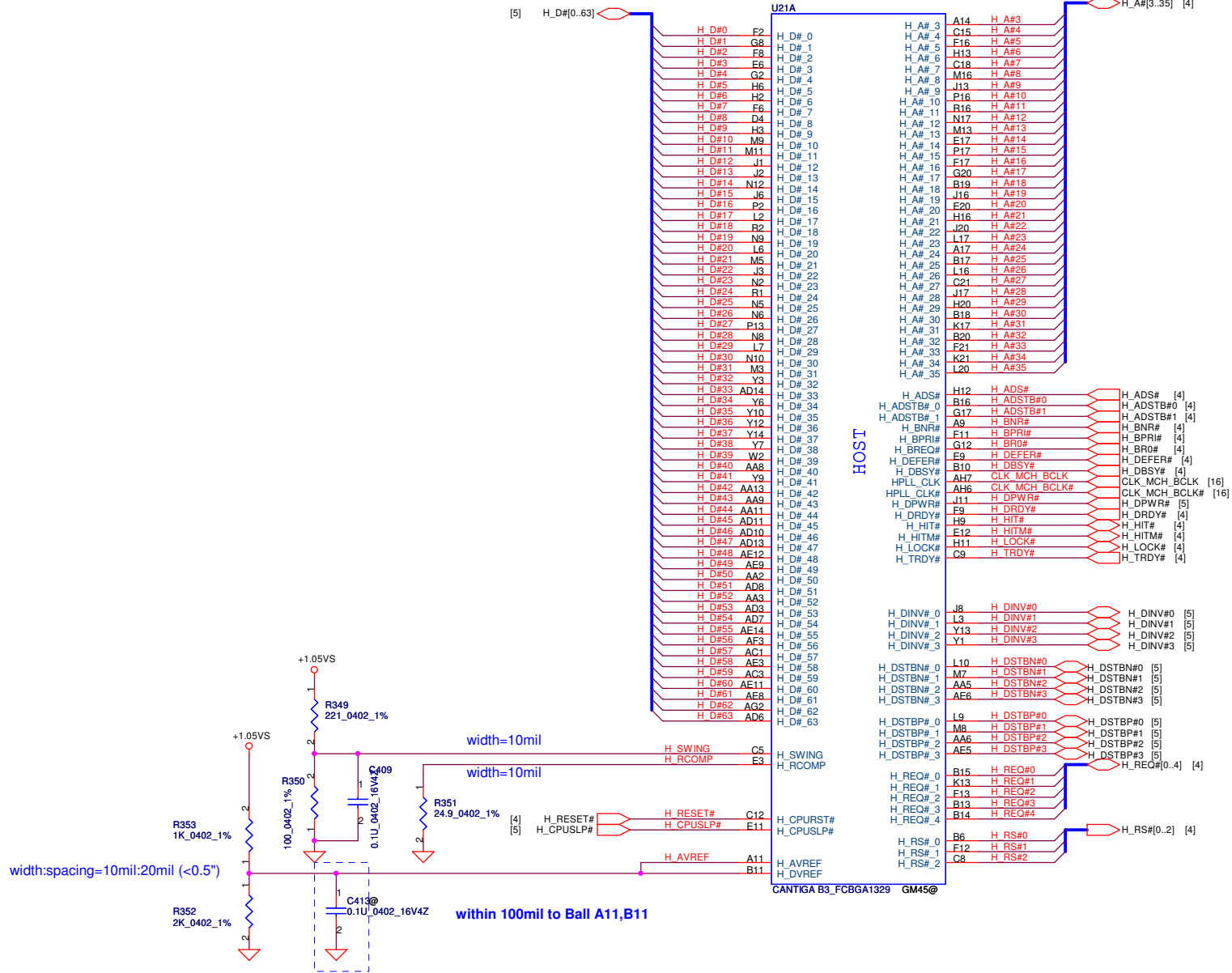


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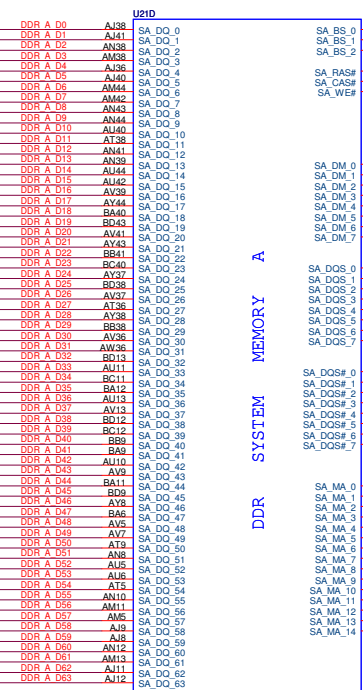


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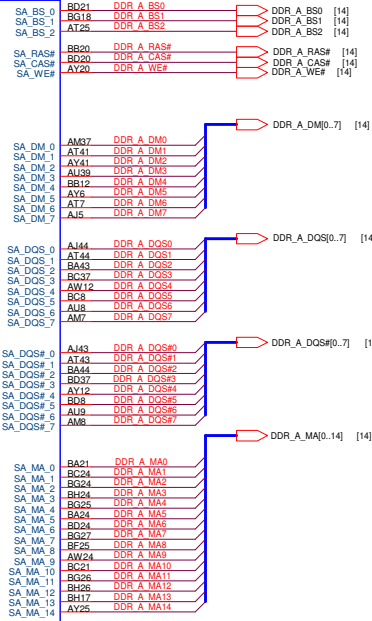


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[14] DDR_A_D[0..63]

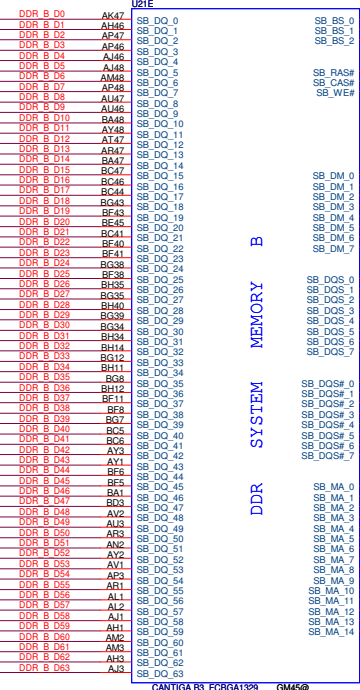


DDR SYSTEM MEMORY A

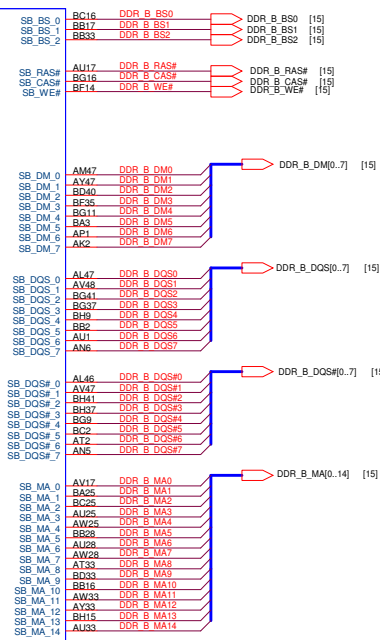


CANTIGA B3_FCBGA1329 GM45@

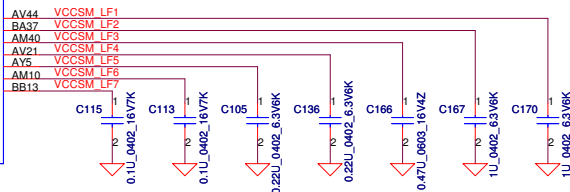
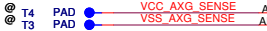
[15] DDR_B_D[0..63]



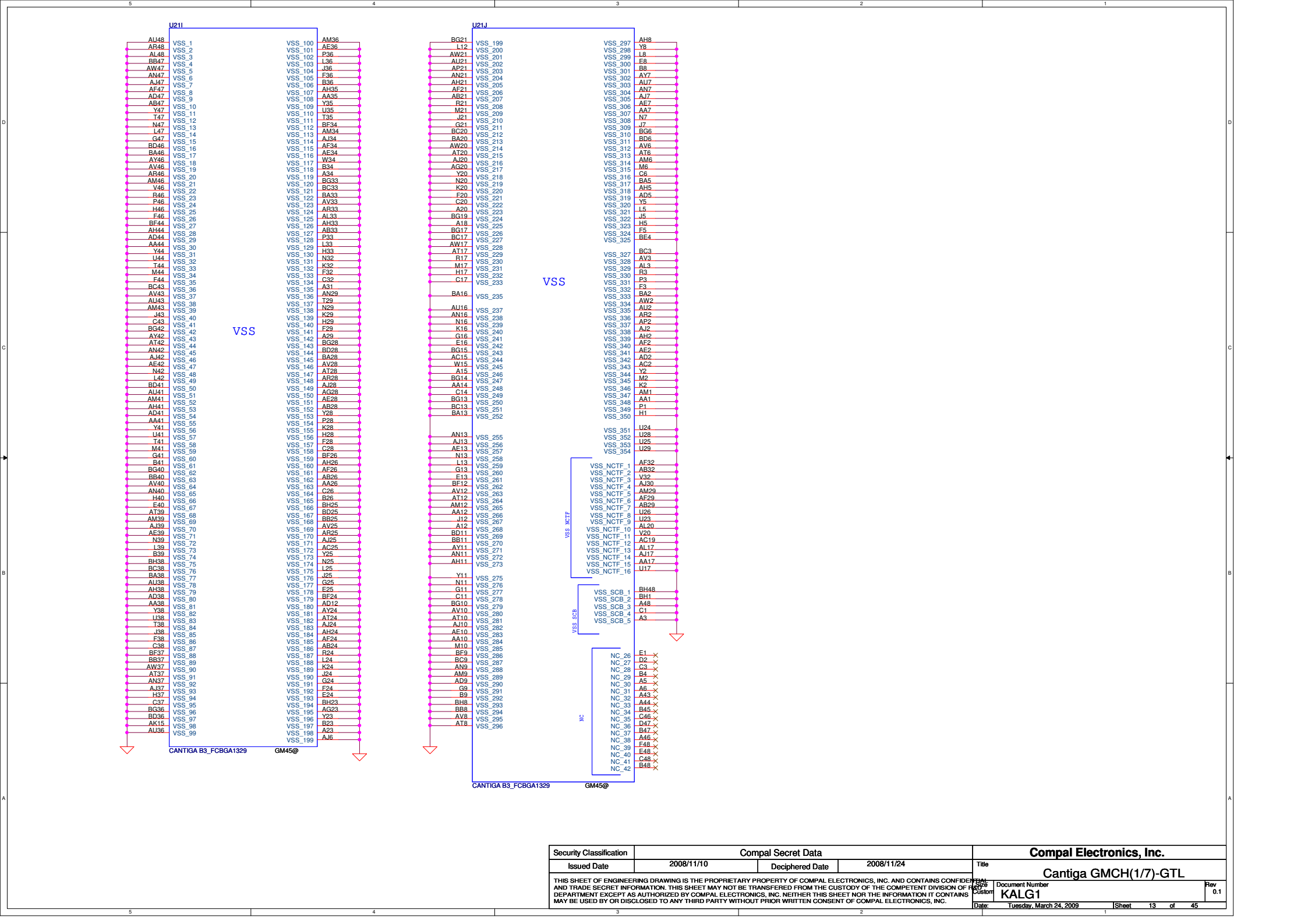
DDR SYSTEM MEMORY B

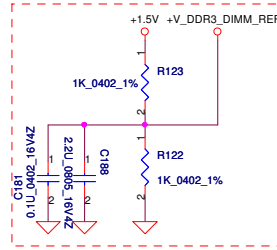
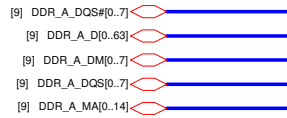


CANTIGA B3_FCBGA1329 GM45@



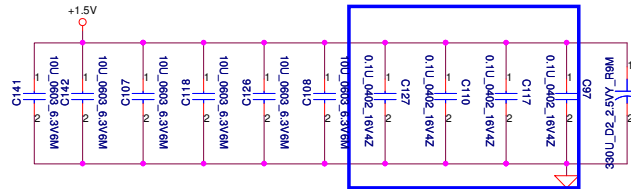
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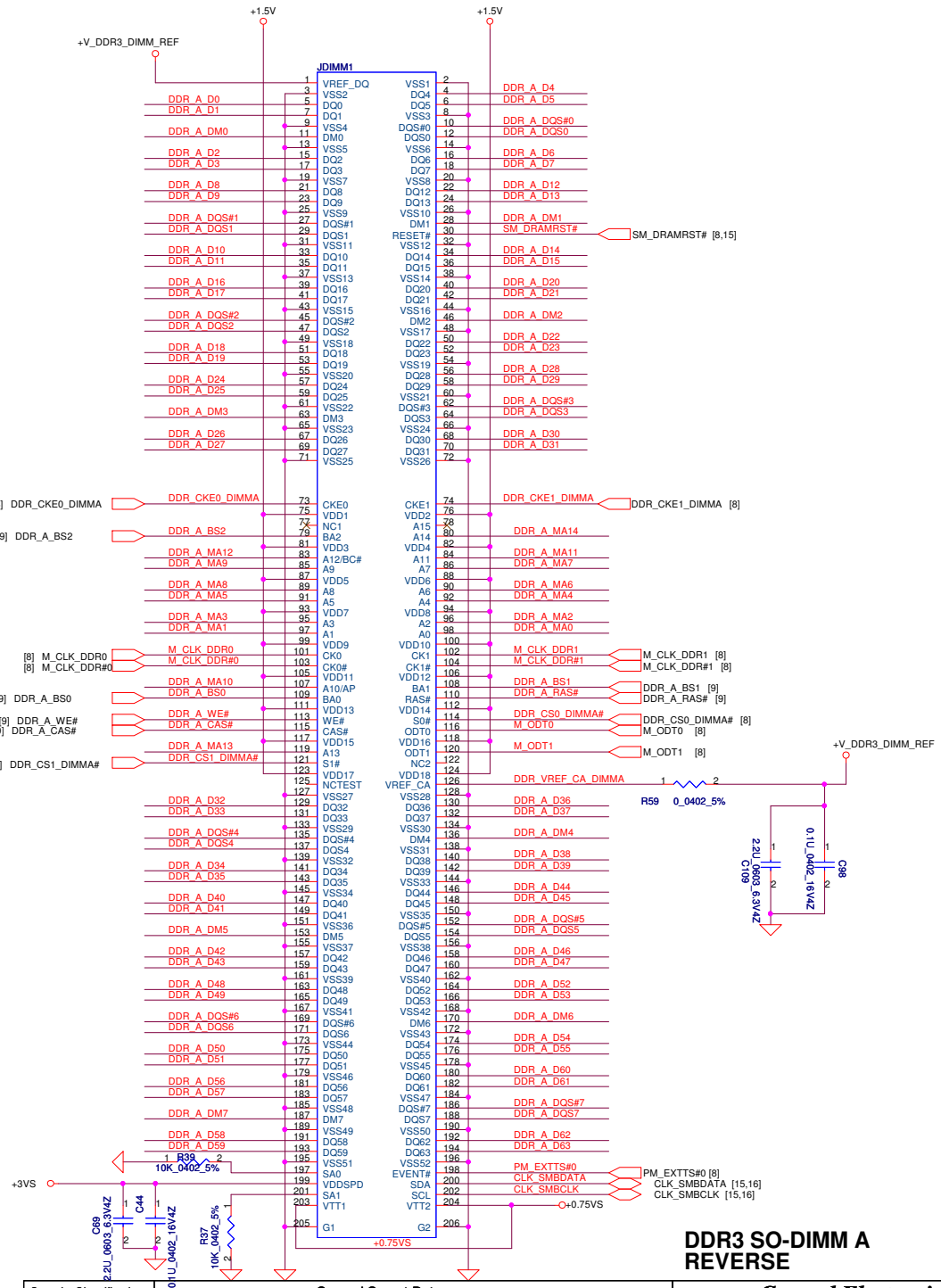
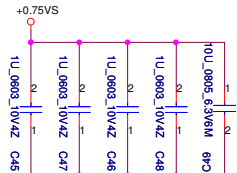


Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA

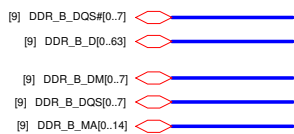


Layout Note:
Place near JP4.203 & JP4.204



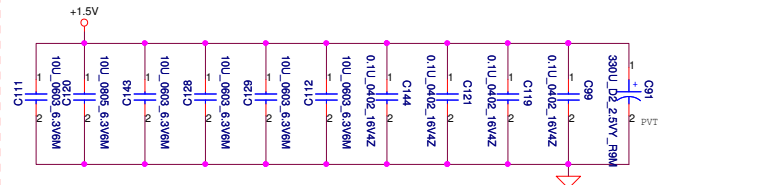
DDR3 SO-DIMM A REVERSE

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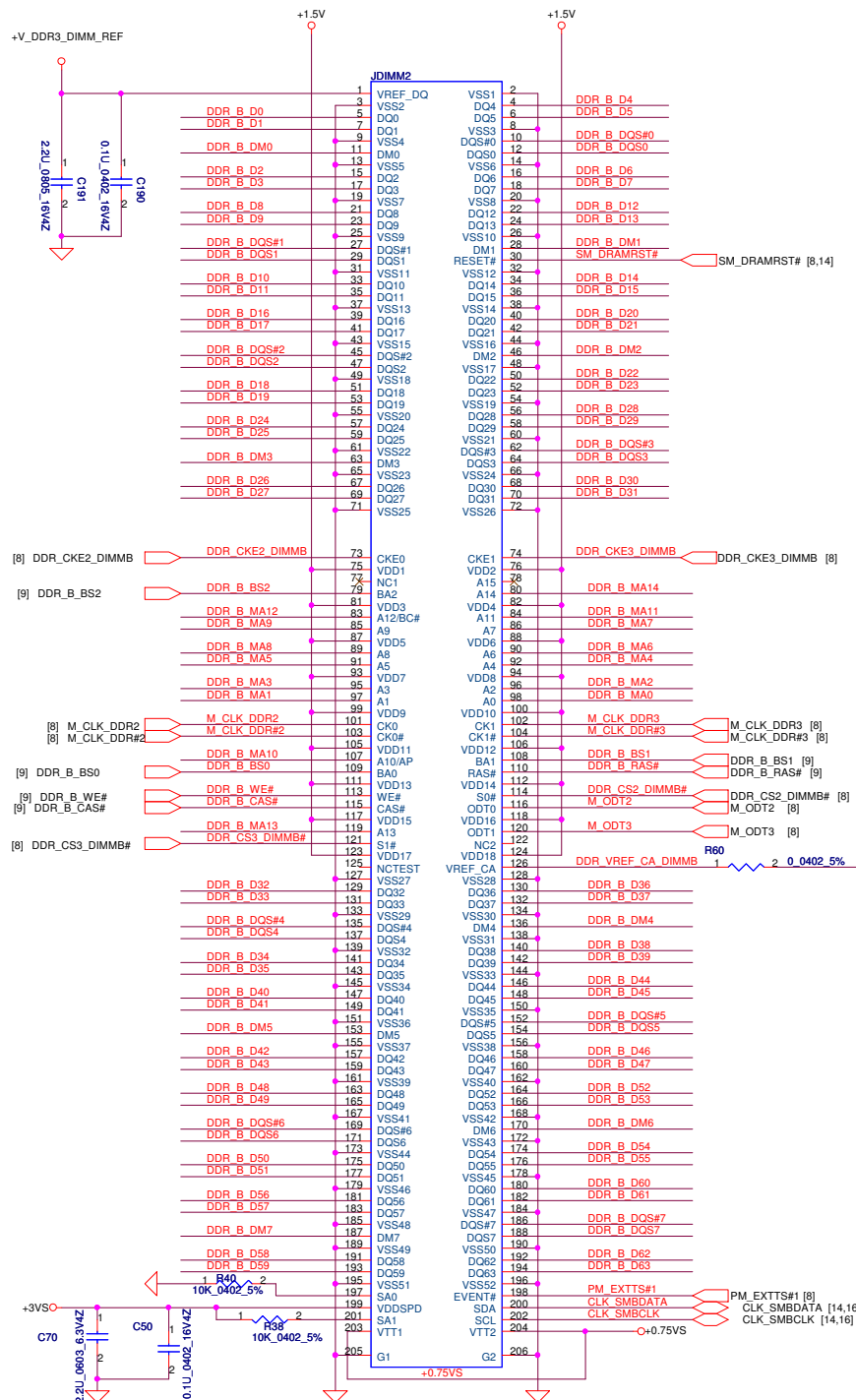
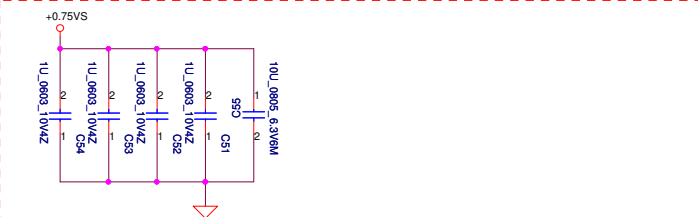


Layout Note:
Place near JP5

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB



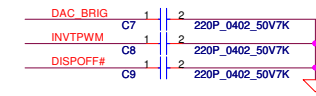
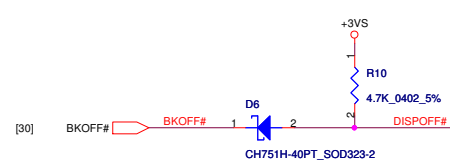
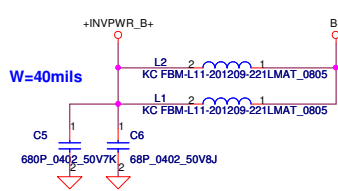
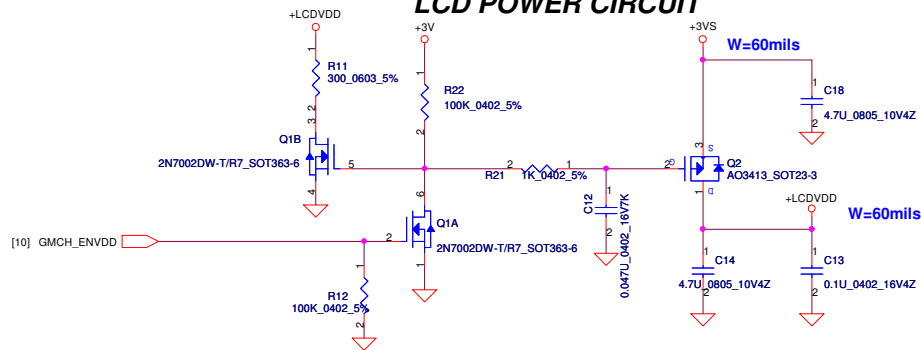
Layout Note:
Place near JP5.203 & JP5.204



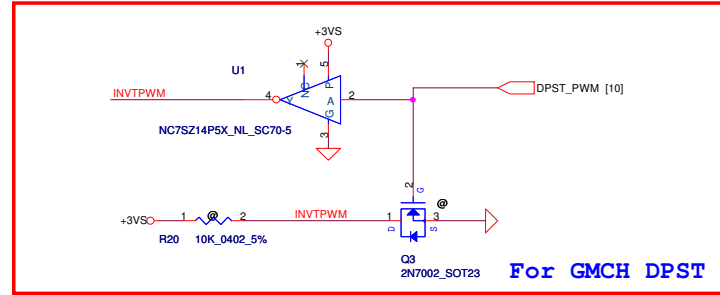
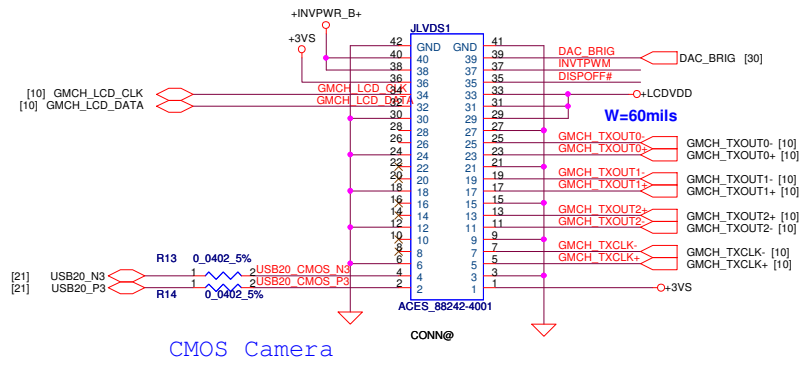
DDR3 SO-DIMM B REVERSE

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LCD POWER CIRCUIT

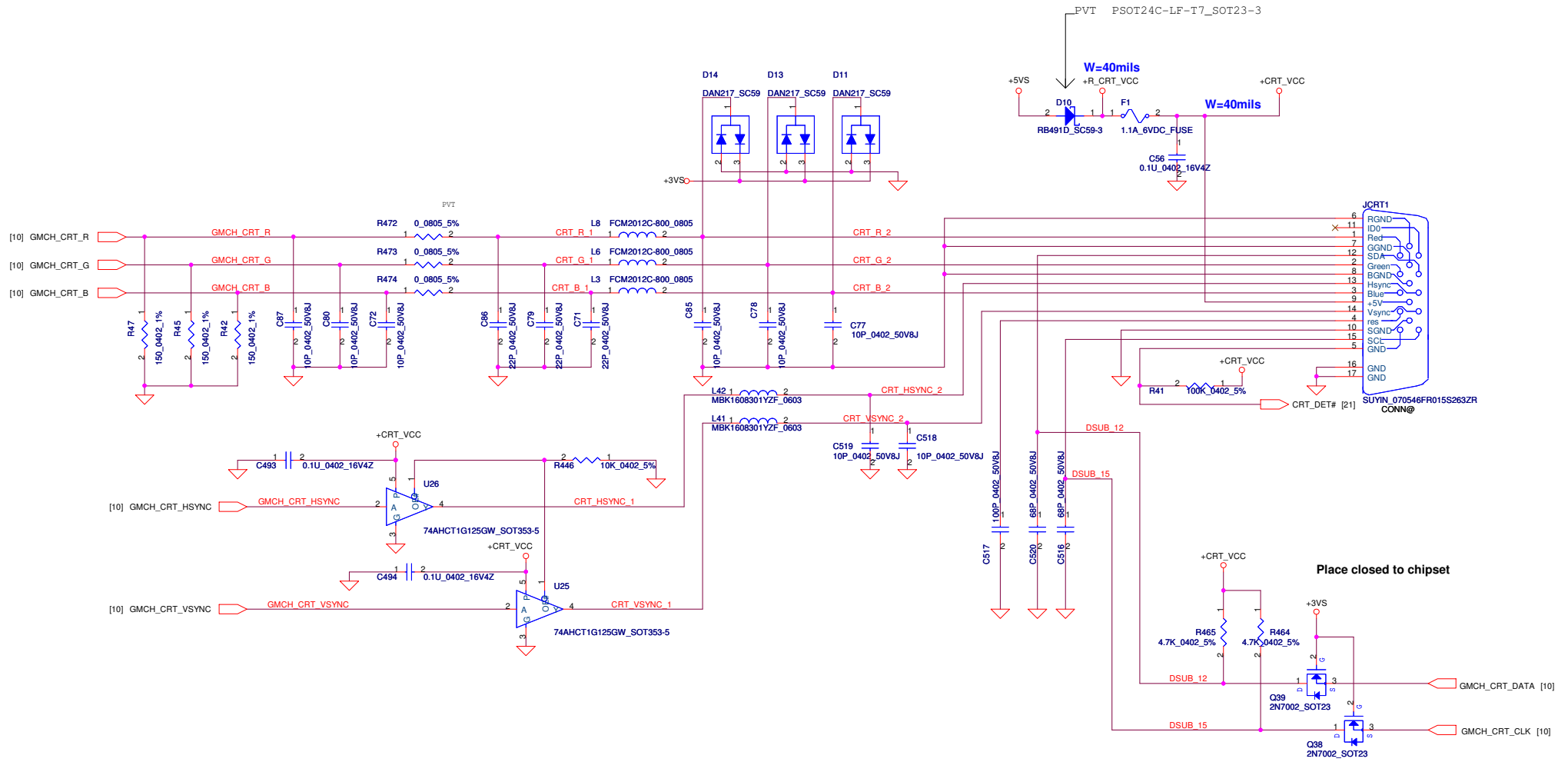


LCD/PANEL BD. Conn.

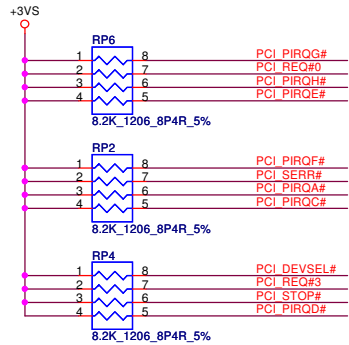
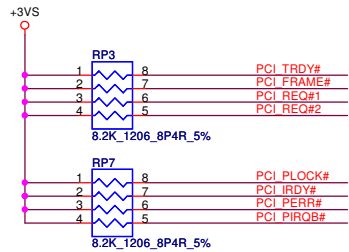


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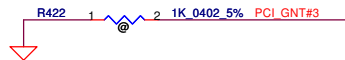
CRT Connector



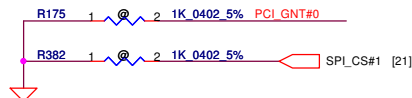
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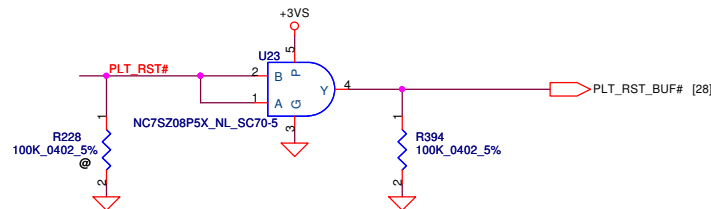
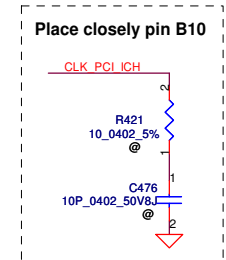
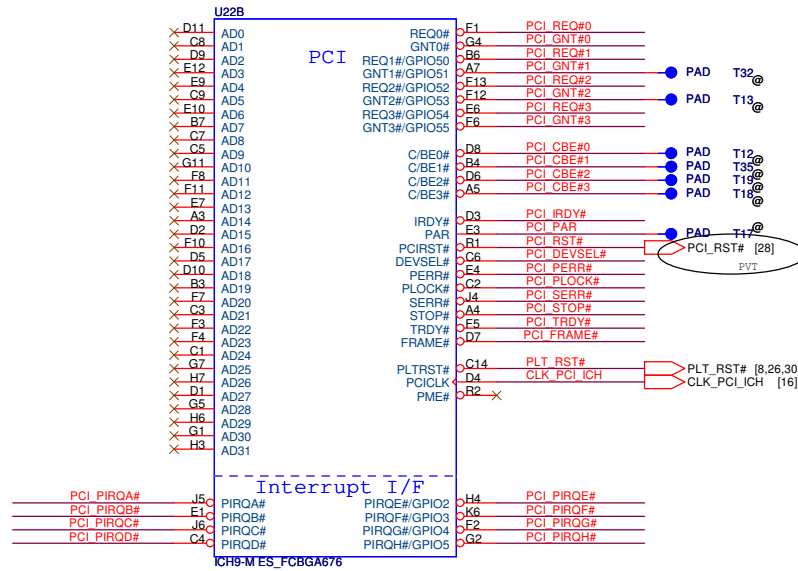
A16 Swap Override Strap
PCI_GNT#3 Low= A16 swap override Enable
 High= Default*



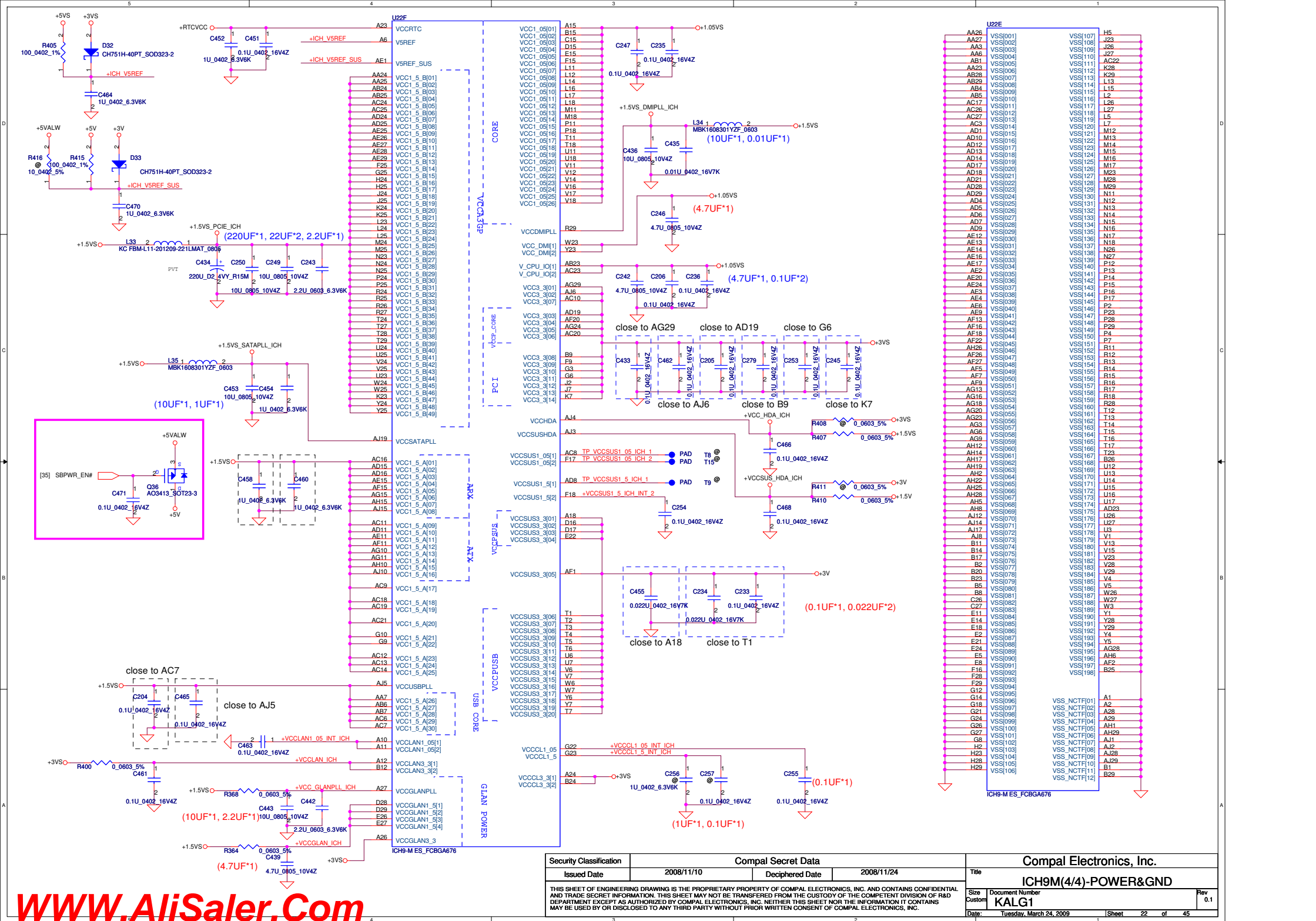
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



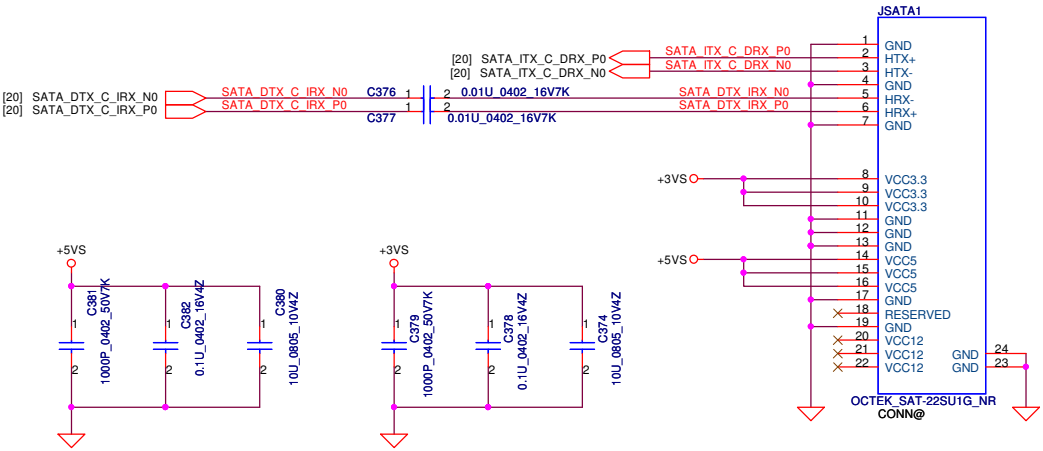
DMI for ESI-compatible operation
PCI_GNT#1 Low= DMI for ESI-compatible operation
 High= Default* (Internal pull-up)



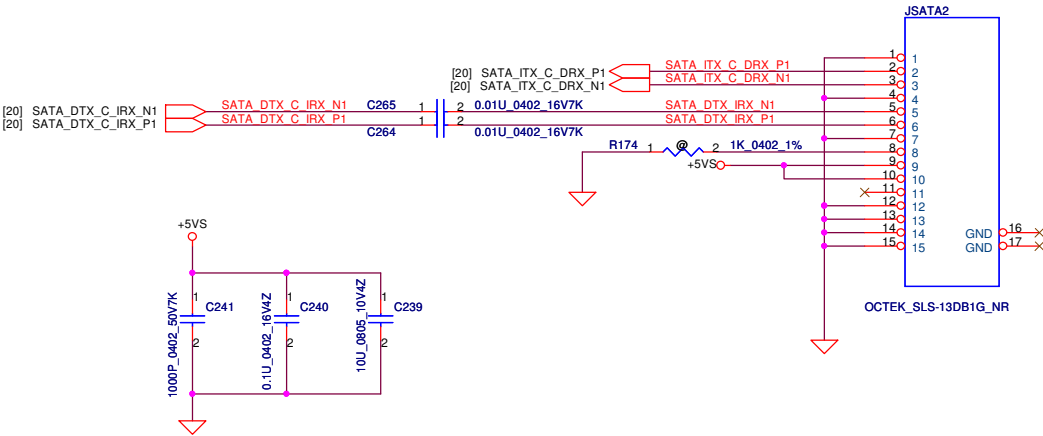
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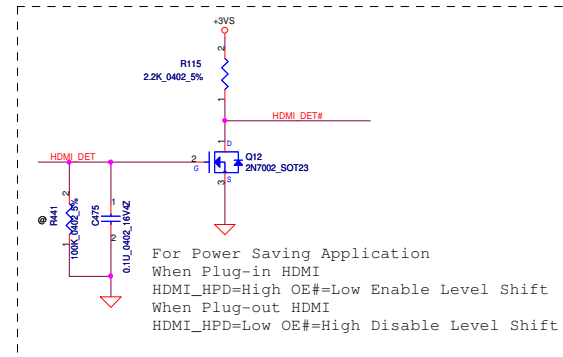
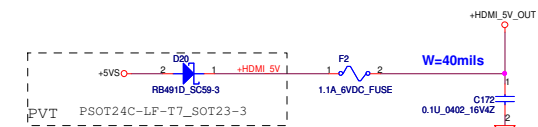
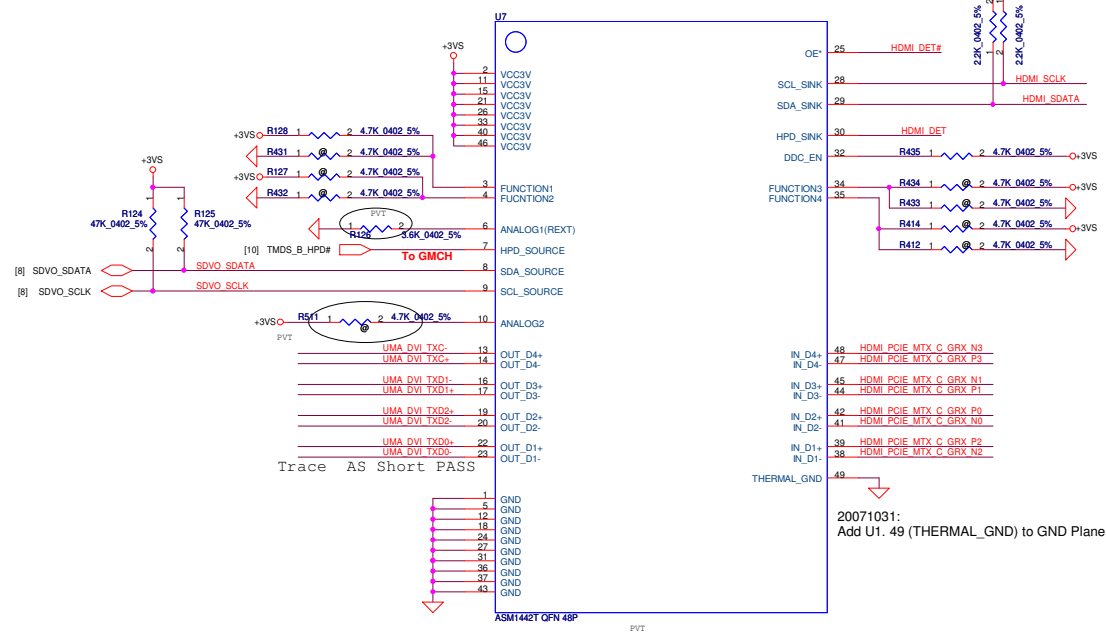
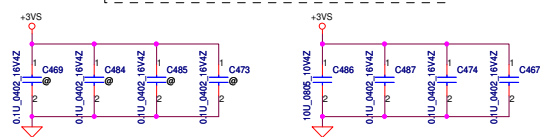
SATA HDD Conn.



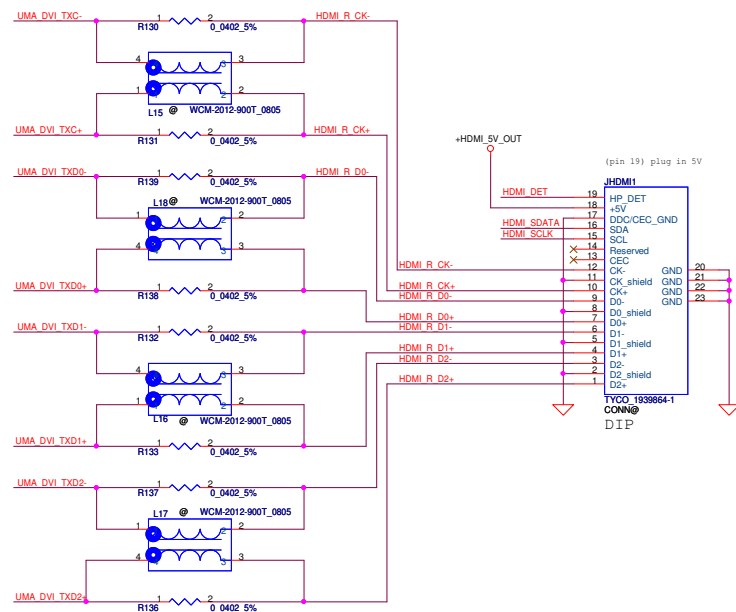
SATA ODD Conn.



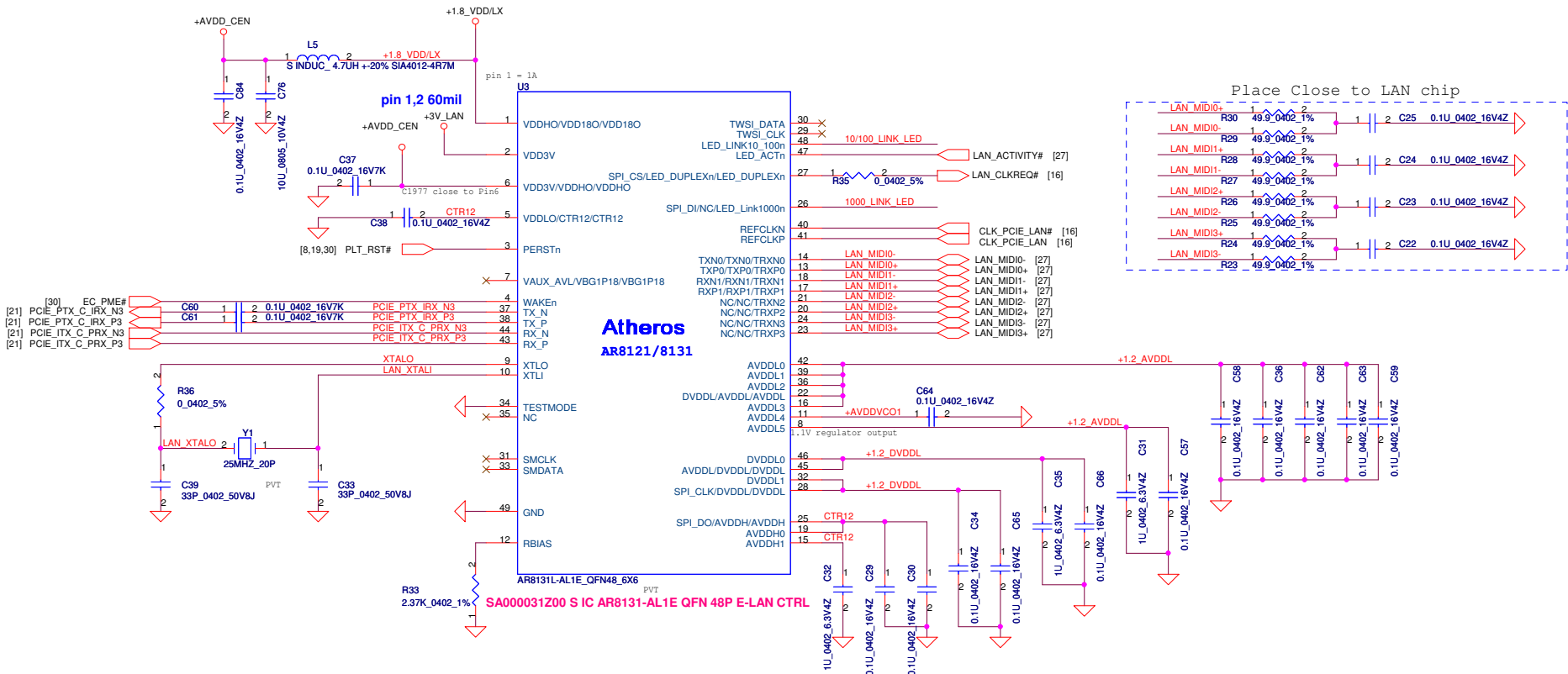
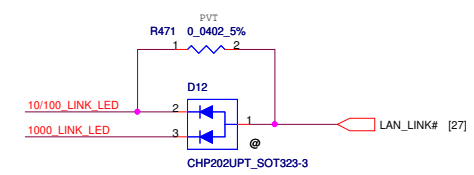
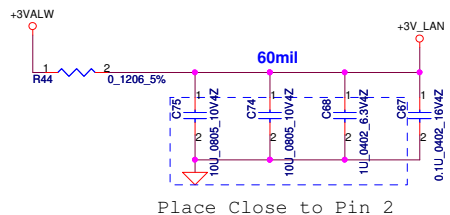
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Issued Date		2008/11/10		Deciphered Date	
2008/11/10		2008/11/24		Title	
HDD & ODD Connector		Size		Document Number	
KALG1		Rev		0.1	
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<u>HDMI_PCIE_MTX_C_GRX_N[0..3]</u>		HDMI_PCIE_MTX_C_GRX_N[0..3]	[10]
<u>HDMI_PCIE_MTX_C_GRX_P[0..3]</u>		HDMI_PCIE_MTX_C_GRX_P[0..3]	[10]

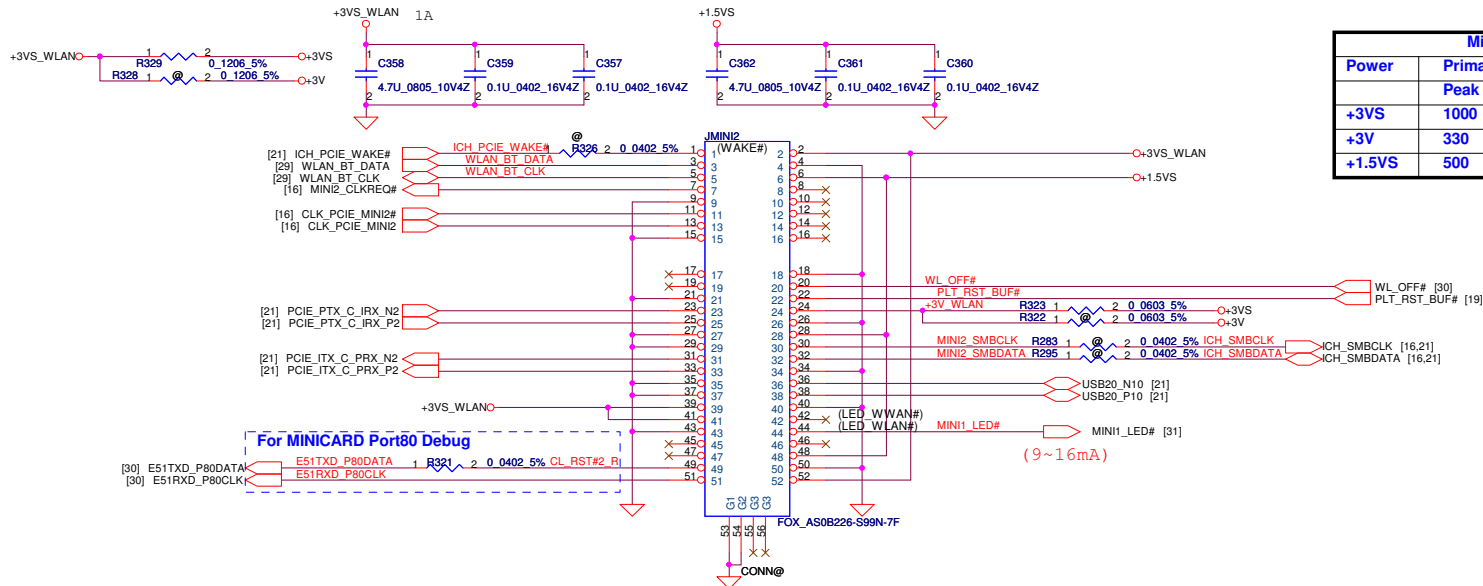


Intel Cantiga TMD5 Pin Definition	
TMD5_B_CLK TMD5_B_CLK#	PEG_TXP_3 PEG_TXN_3
TMD5_B_DATA0 TMD5_B_DATA0#	PEG_TXP_2 PEG_TXN_2
TMD5_B_DATA1 TMD5_B_DATA1#	PEG_TXP_1 PEG_TXN_1
TMD5_B_DATA2 TMD5_B_DATA2#	PEG_TXP_0 PEG_TXN_0
TMD5_B_HPD#	PEG_RXP_3



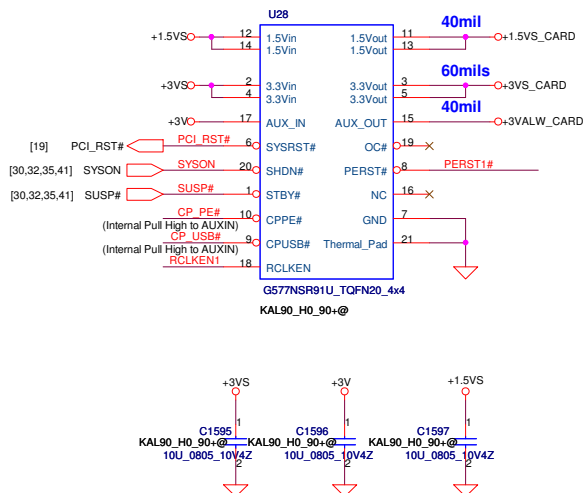
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2008/04/16				Atheros AR8131			
Deciphered Date				2008/11/24				KALG1			
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For Wireless LAN

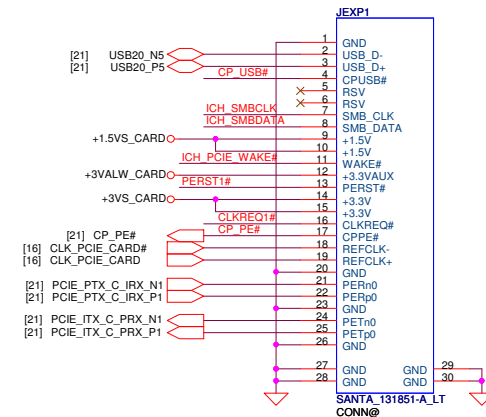


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

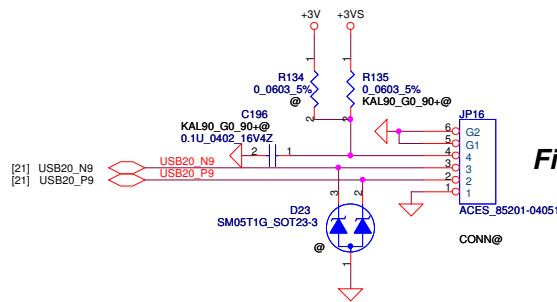
New Card Power Switch



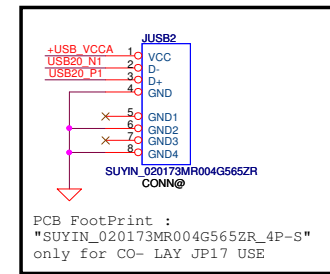
New Card Socket (Left/TOP)



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				Date	Tuesday, March 24, 2009
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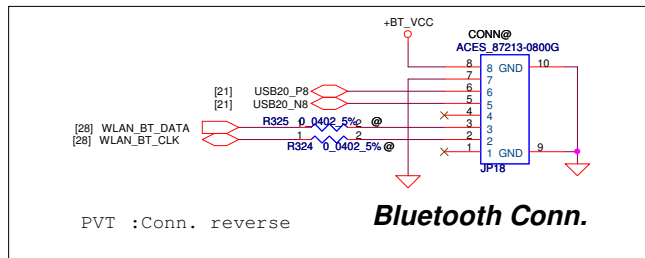
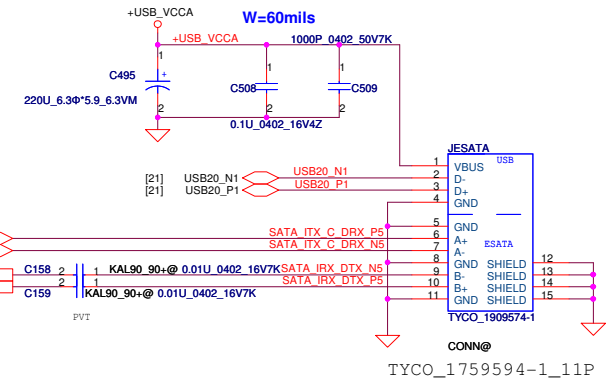
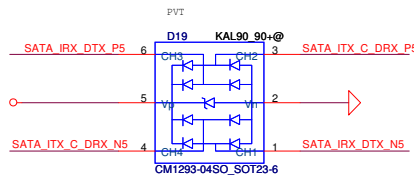
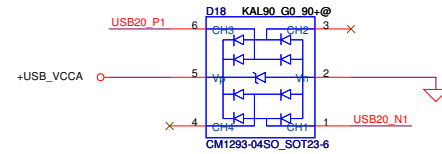
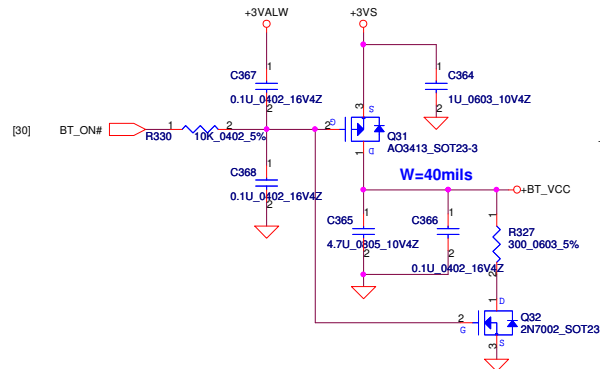


Finger Print Conn.

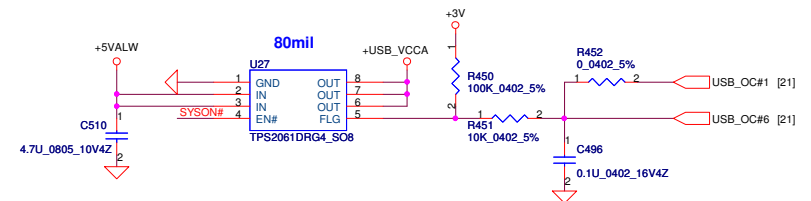


PCB FootPrint :
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only for CO- LAY JP17 USE

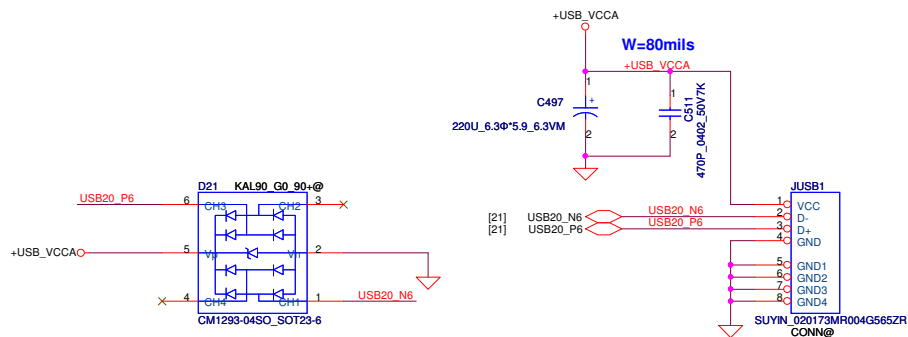
ESATA CONN



Bluetooth Conn.



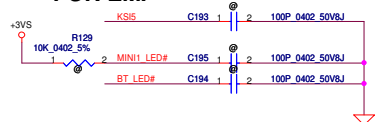
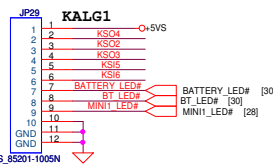
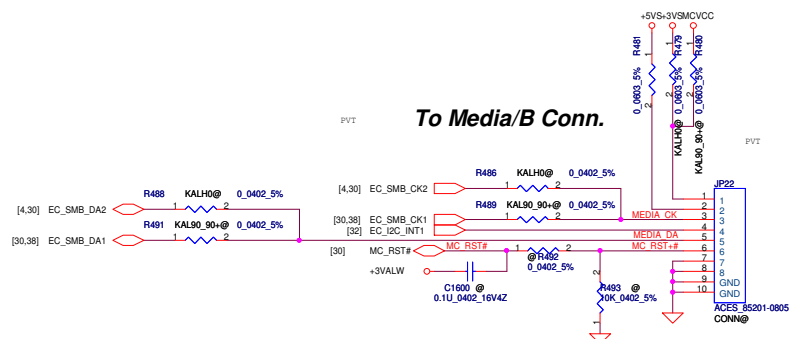
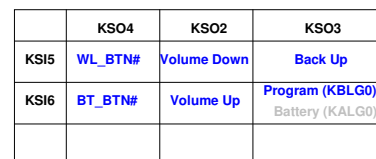
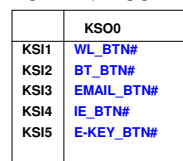
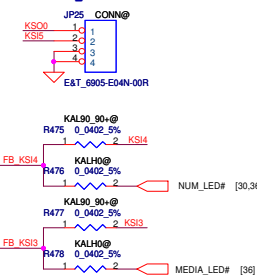
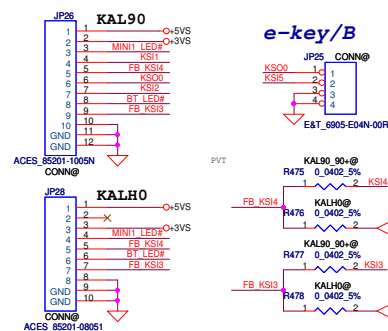
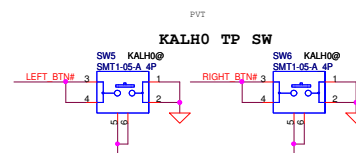
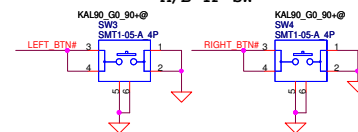
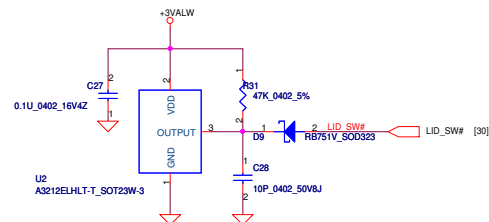
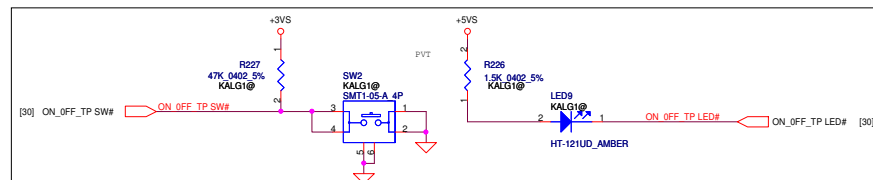
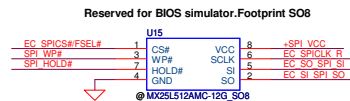
To USB/B Connector



USB CONN.

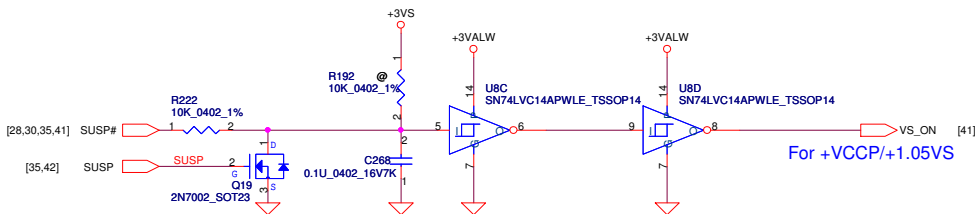
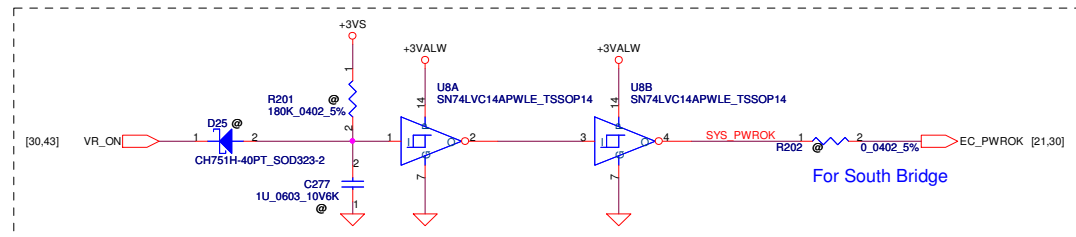
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								Document Number		Rev	
								KALG1		0.1	
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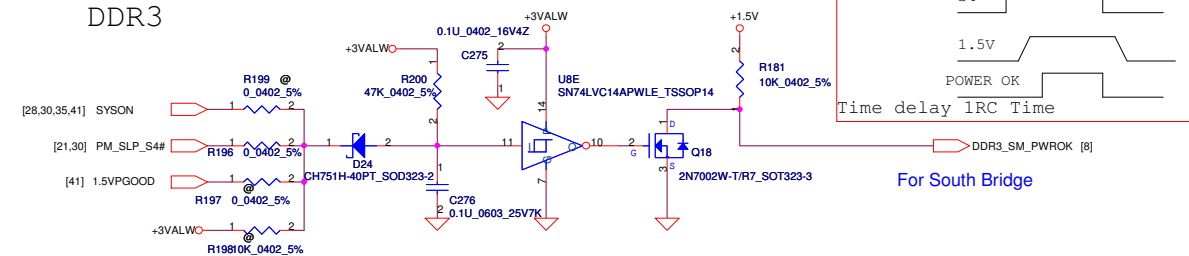


	Compaq Electronics, Inc.
Title	BIOS, I/O Port & K/B Connector

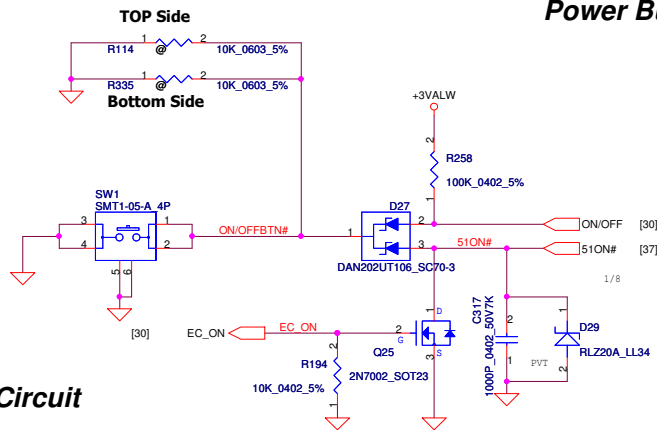
Power ON Circuit



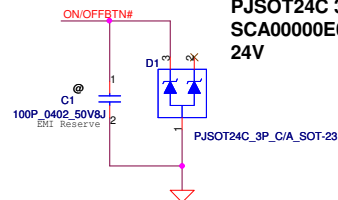
DDR3



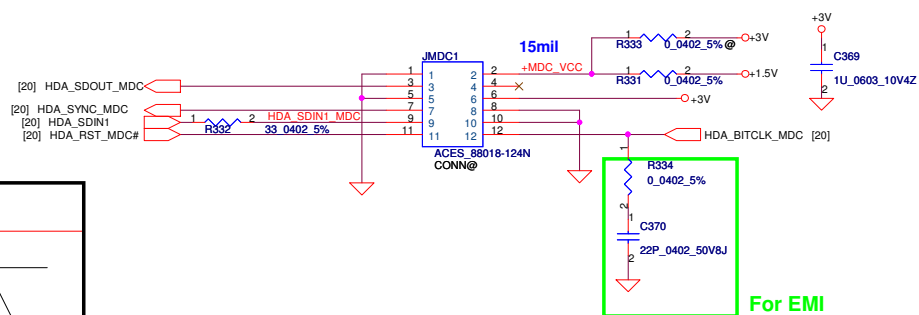
Power Button



D58 USE
PJSOT24C 3P C/A SOT-23
SCA00000E00
24V

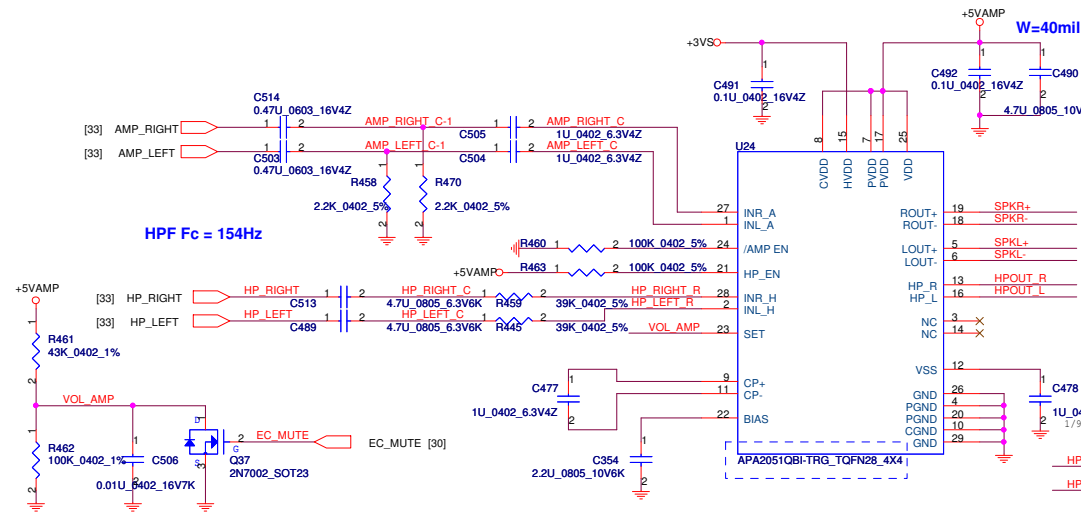


HDA MDC Conn.

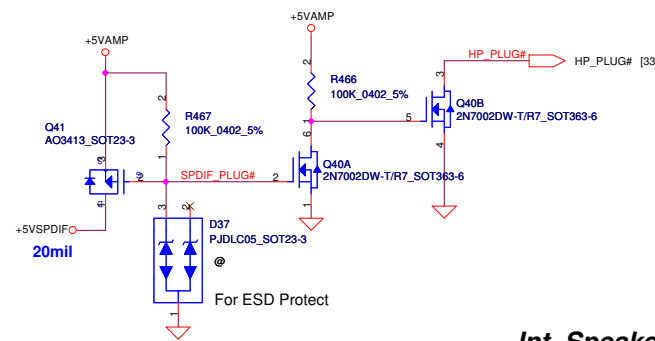
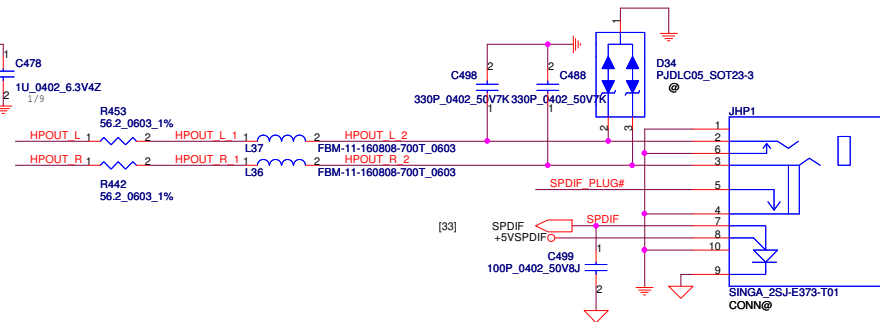


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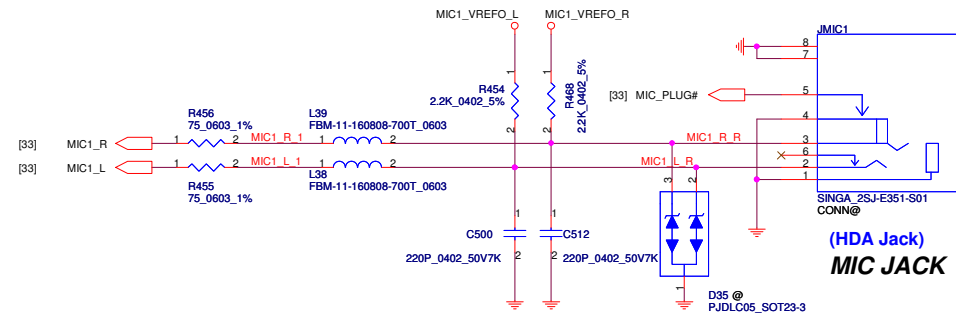
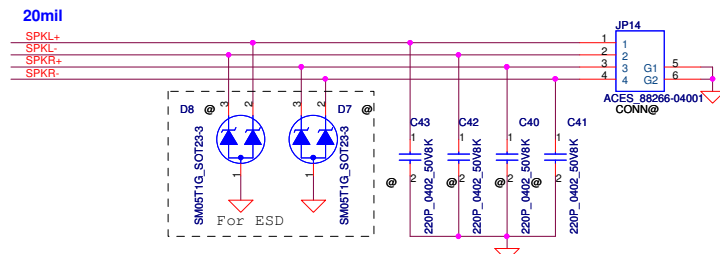
Gain= 10dB



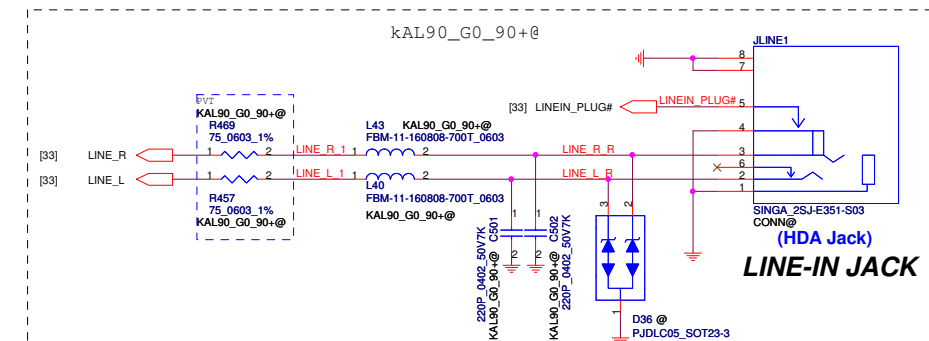
S/PDIF Out JACK
LINE Out/Headphone Out



Int. Speaker Conn.



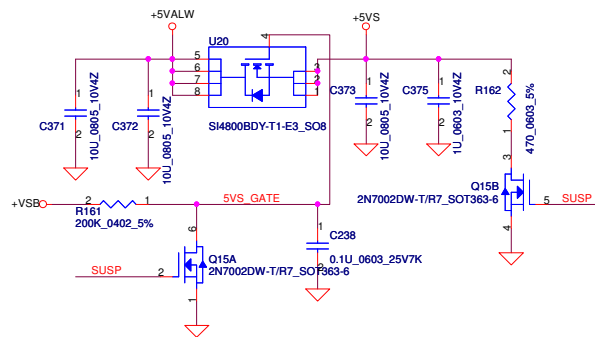
(HDA Jack)
MIC JACK



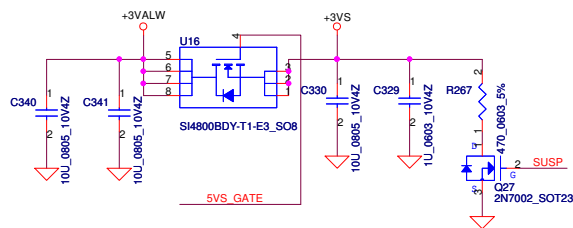
(HDA Jack)
LINE-IN JACK

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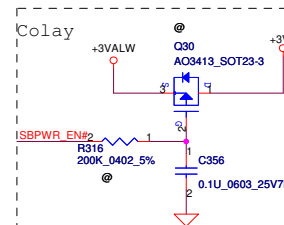
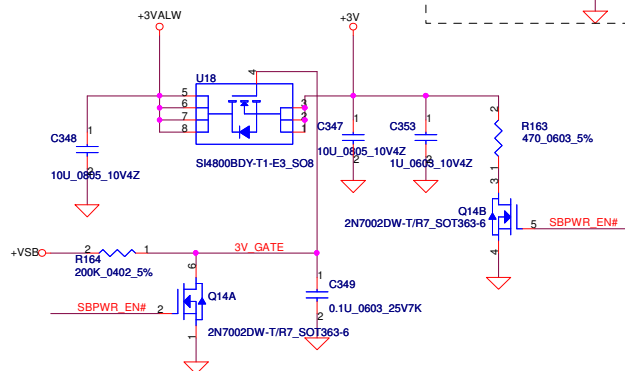
+5VALW TO +5VS



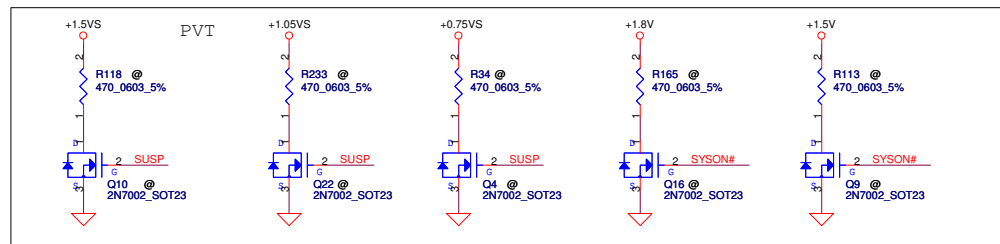
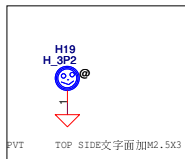
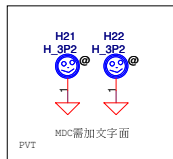
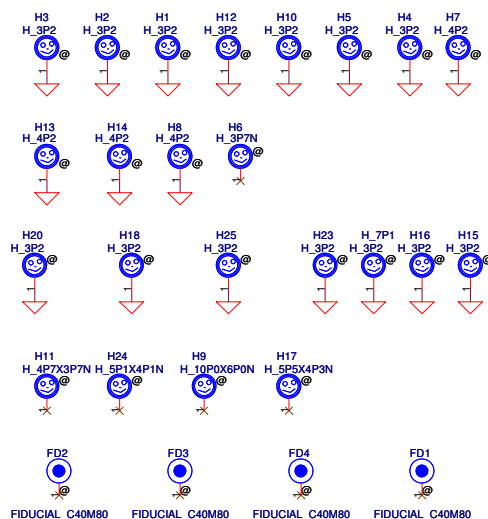
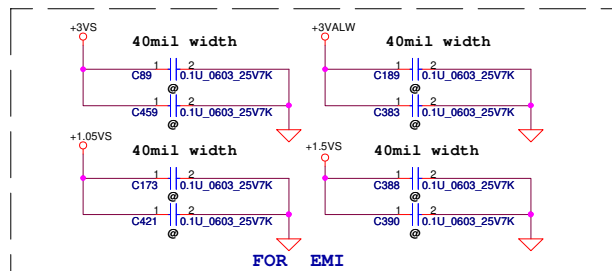
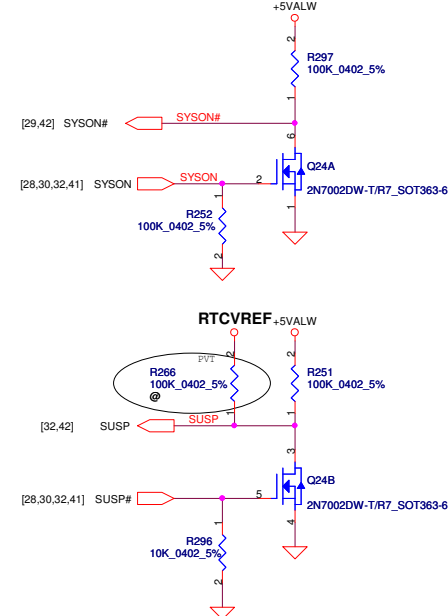
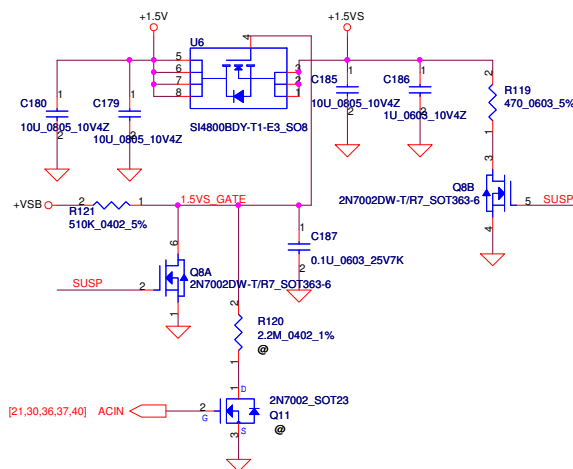
+3VALW TO +3VS



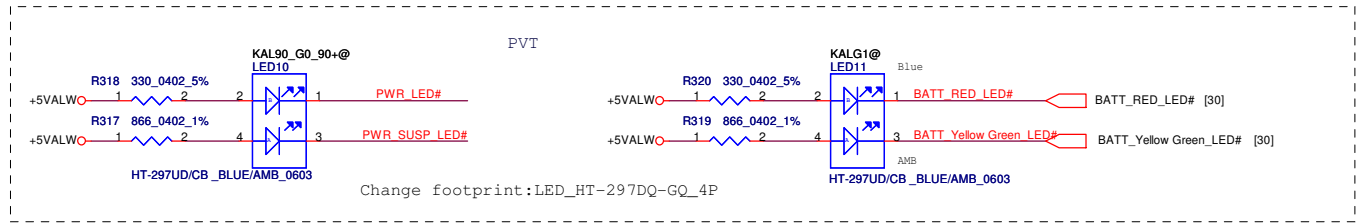
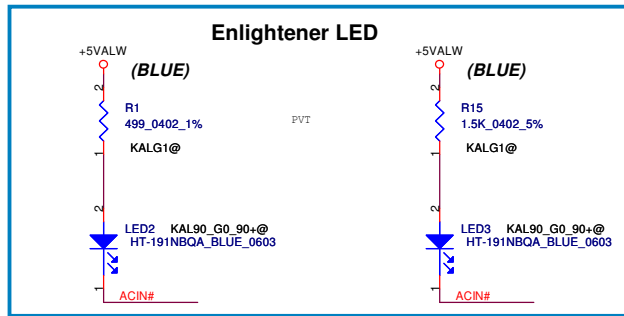
+3VALW TO +3V_SB(ICH8M AUX Power)



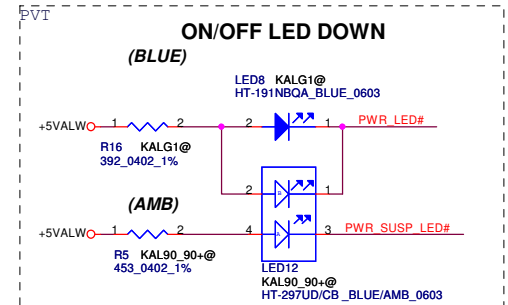
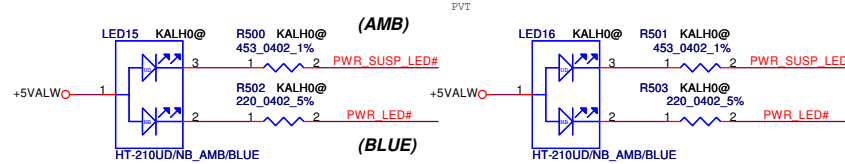
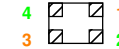
+1.5V to +1.5VS



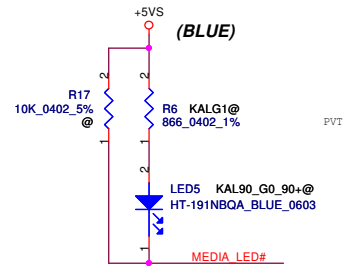
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								DC Interface & Screw Hole					
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Rev													
Date								Tuesday, March 24, 2009		Sheet 35 of 45			



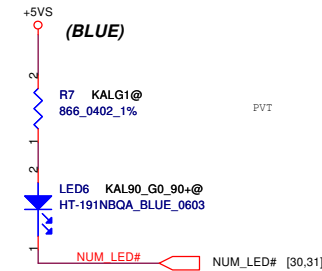
Compal Footprint



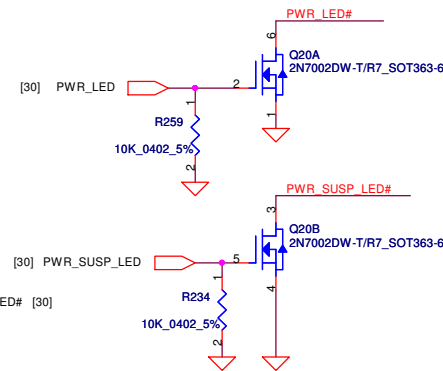
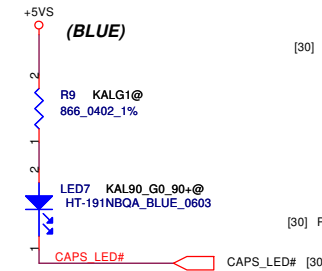
MEDIA_LED



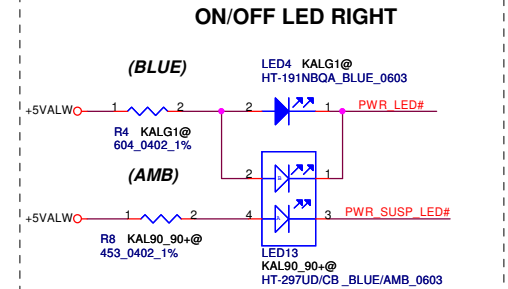
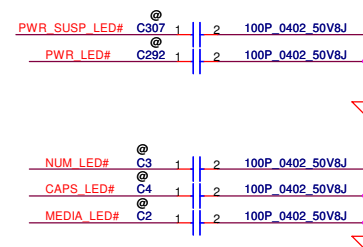
NUM_LED



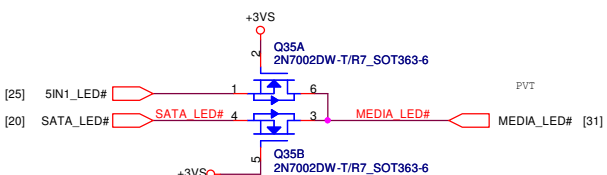
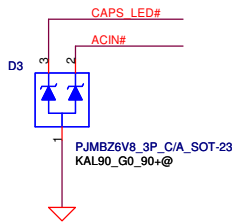
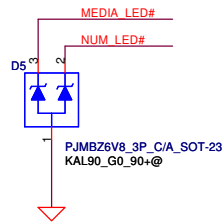
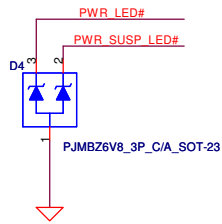
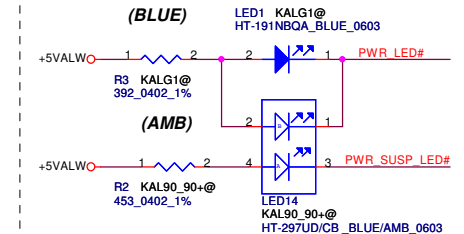
CAPS_LED



FOR EMI

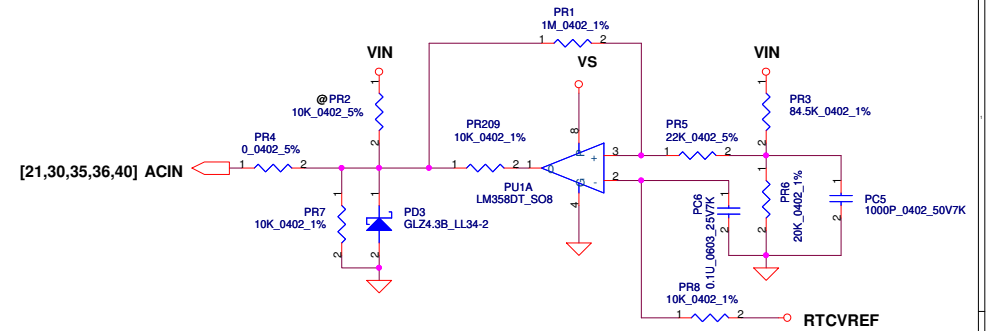
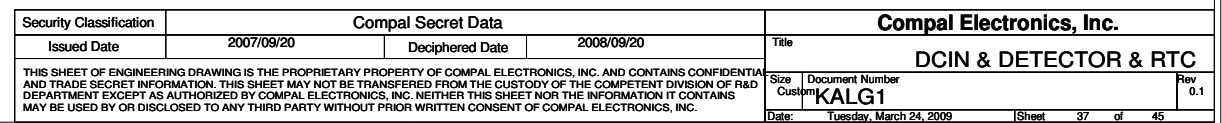
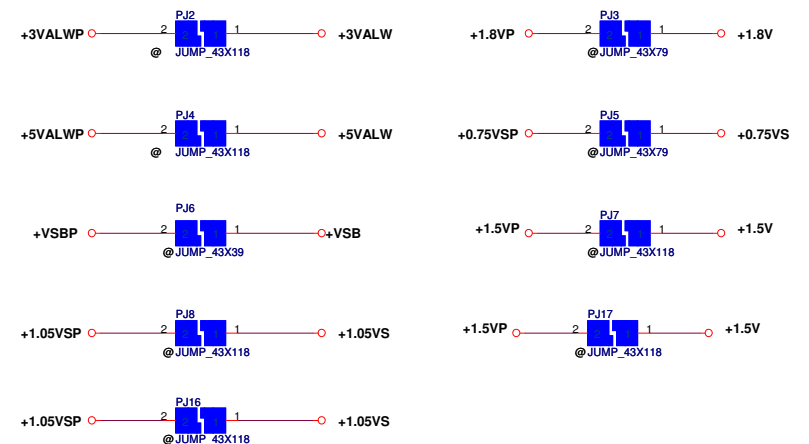


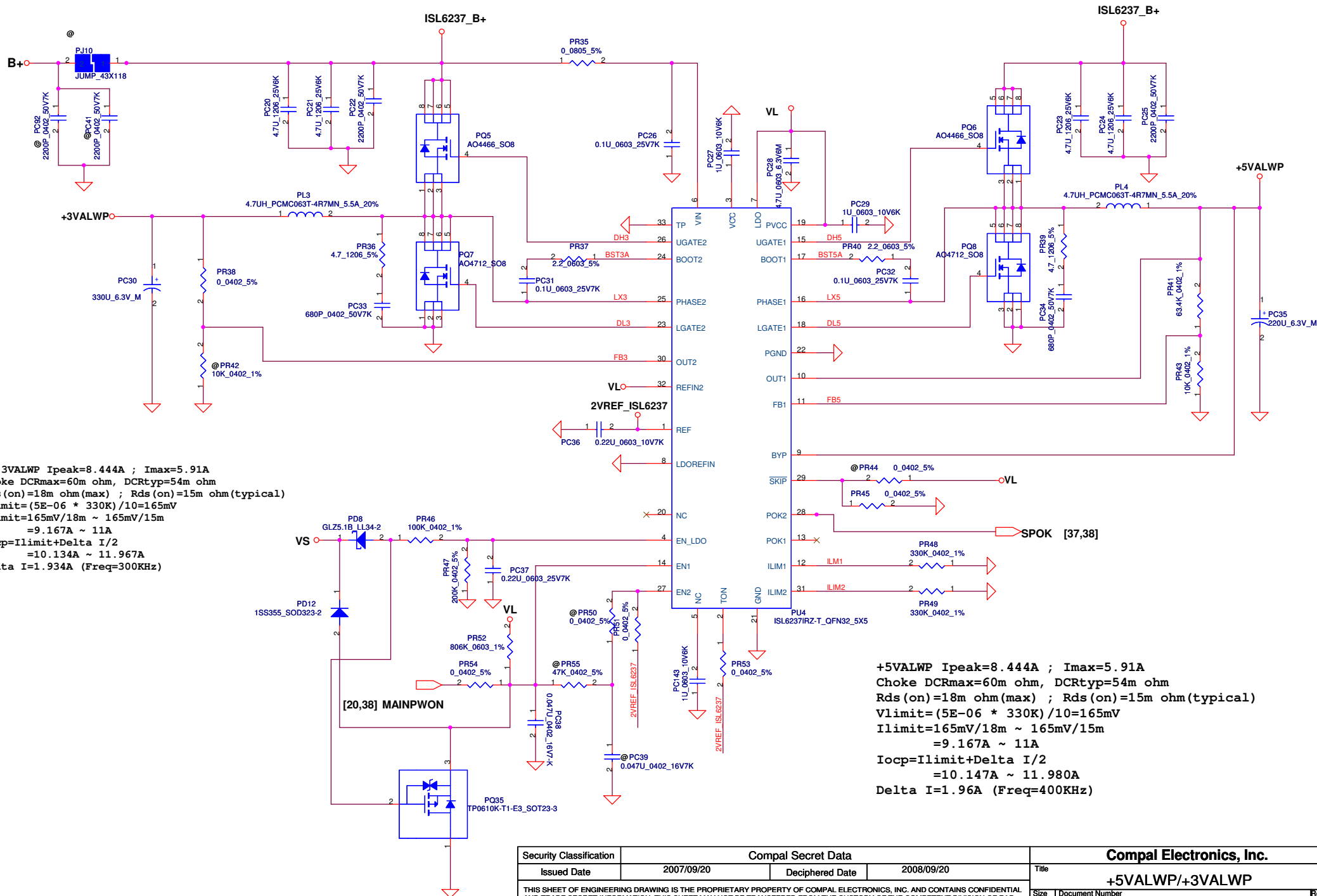
ON/OFF LED LEFT



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SINGA 2DC-G756I200

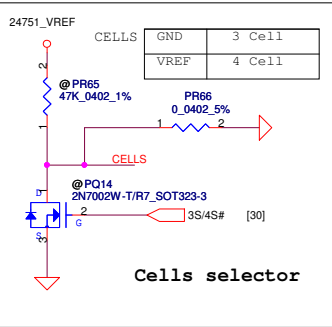
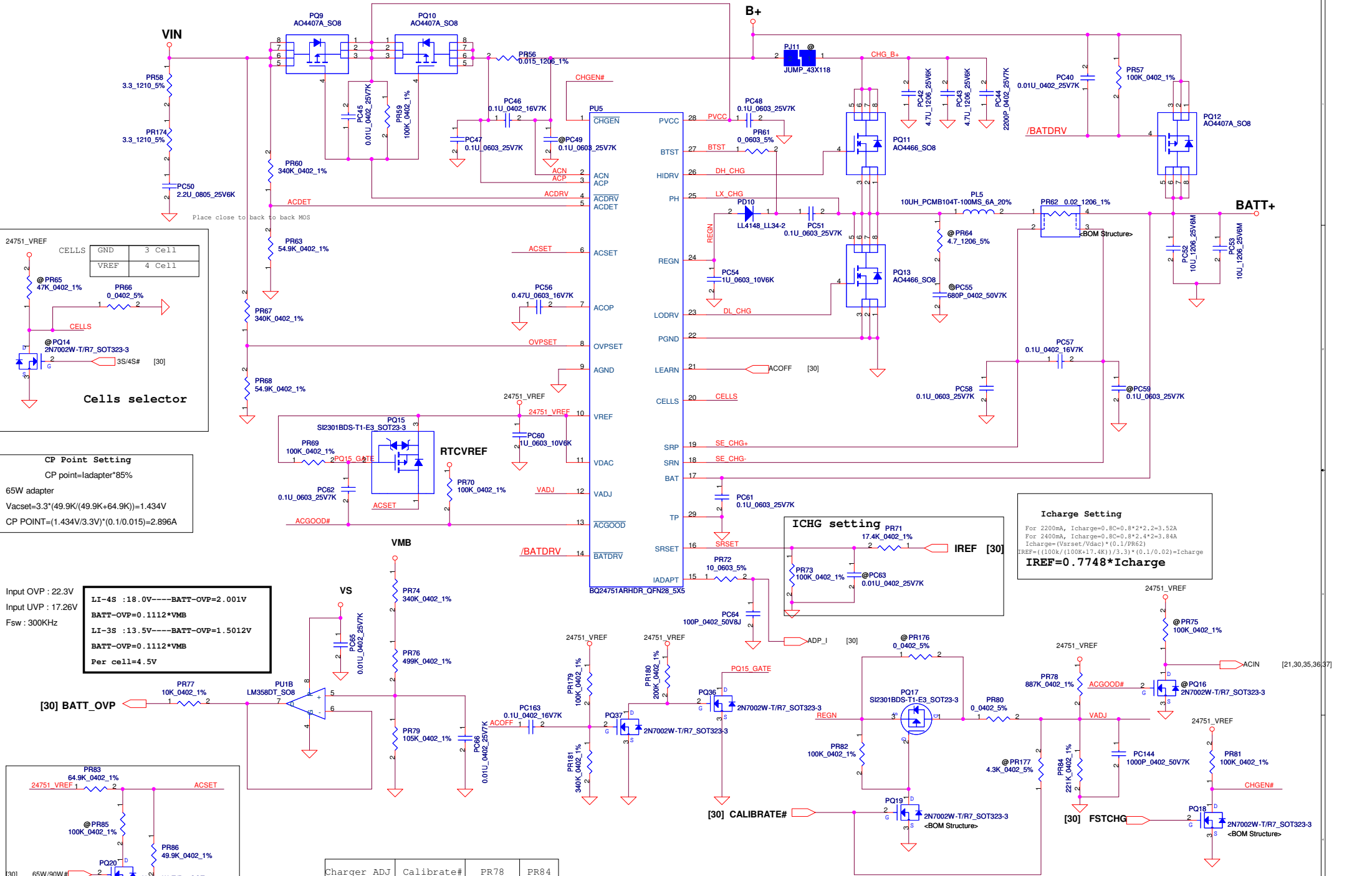
RTC Conn



+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.134A ~ 11.967A
Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.96A (Freq=400KHz)

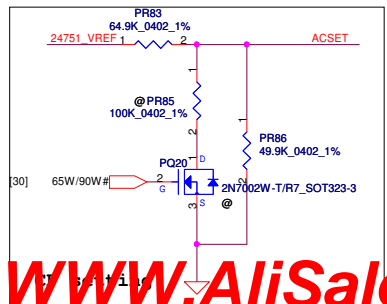
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CP Point Setting
CP point=ladapter*85%
65W adapter
Vacset=3.3*(49.9K/(49.9K+64.9K))=1.434V
CP POINT=(1.434V/3.3V)*(0.1/0.015)=2.896A

Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz

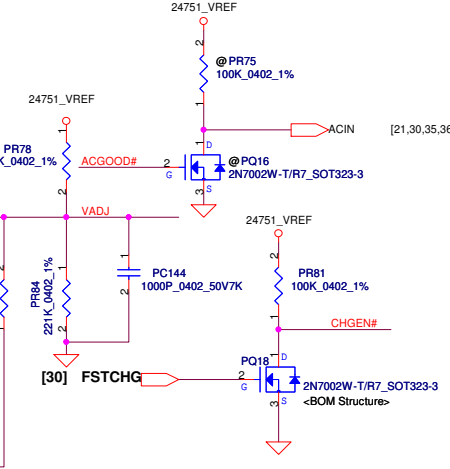
LI-4S : 18.0V----BATT-OVP=2.001V
BATT-OVP=0.1112*VMB
LI-3S : 13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=4.5V



Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
	H	@	@

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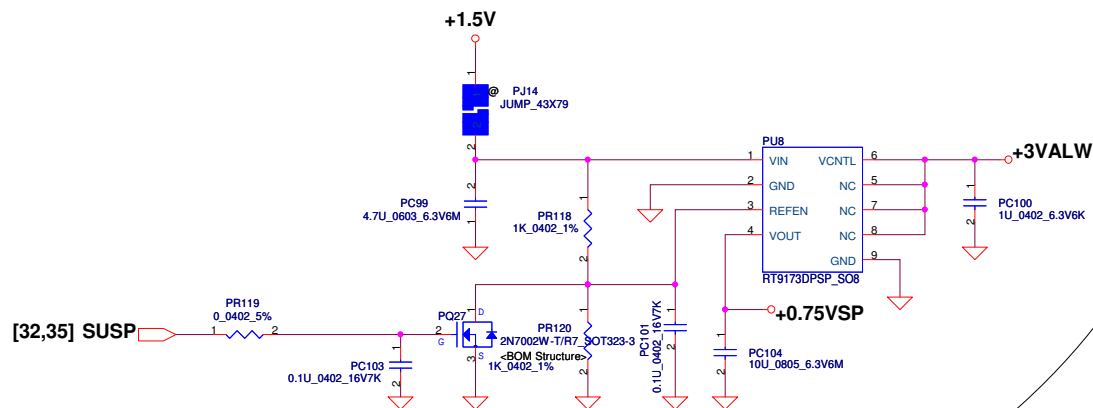
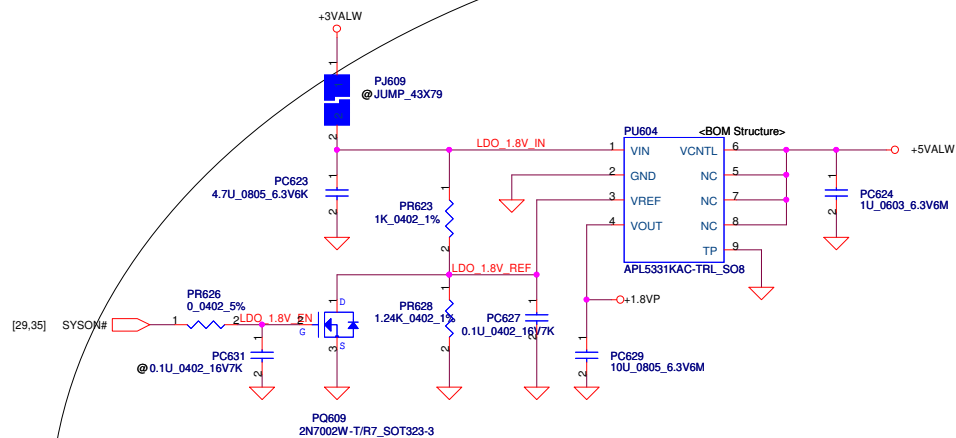
Icharge Setting
For 2200mA, Icharge=0.8*(0.8*2*2.2+3.52A)
For 2400mA, Icharge=0.8*(0.8*2.4*2+3.84A)
Icharge=(Varset/Vdac)*(0.1/PR62)
IREF=(100k/(100k+17.4K))/3.3*(0.1/0.02)=Icharge
IREF=0.7748*Icharge



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CHARGER	
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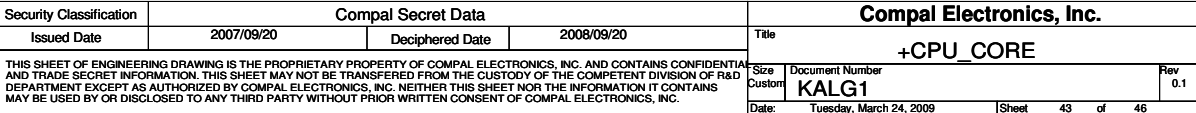


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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Add 3/5V boost resister for EMI request			Change PR37 and PR40 to 2.2 OHM		
2		Modify 1.5V and 1.05V choke to cyntec for eff.			PL501 & PL502		
3		Modify 1.5V and 1.05V frequnce from 336K to 264K for eff.			Change PR525 & PR501 from 240K to 300K		
4		Modify 1.5V and 1.05V low side mos for eff.			Change PQ506 & PQ508 from FDS6670 to A04456		
5		Add CPU_core boost resister for EMI request			Change PR138 and PR158 to 2.2 OHM		
6		Modify 1.5V & 1.05V OCP to 14A			Change PR530 & PR522 to 5.9K		
7		Modify 3V & 5V choke to 4.7UH for eff.			Change PL3 & PL4 from 8.2UH to 4.7UH		
8		Modify 5V output cap to OS-CON for costdown			Change PC35		
9		Modify 3V output cap to OS-CON for costdown			Change PC30		
10		Modify dischager mos to A04407A for rating risk			Change PQ12		
11		Add 30K OHM to TPS51117 EN pin , Disable SMPS mode			ADD PR910 & PR911		
12							
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PCB



LA-5271P MB Rev0: DA60000C500

PCB 08Y LA-5271P REV0 M/B

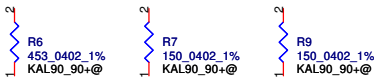
North Bridge



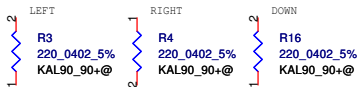
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S IC AC82GL40 SLGGM A1 FCBGA1329 GL ABO
GL40@

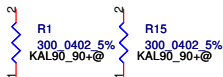
MEDIA_LED NUM_LED CAPS_LED



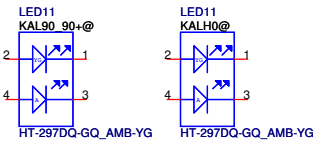
ON/OFF LED Risiter



Enlightener LED



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